Dual-Input Single-Output DC-DC Conversion for Common-Mode Current Suppression in Misaligned Resonant Capacitive Power Transfer Systems

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***Abstract*—A dual-input single-output DC-DC is proposed to reduce common-mode currents in laterally misaligned resonant capacitive power transfer systems, thereby mitigating shield voltage rise and electromagnetic emissions without compromising power sharing or efficiency. Simulations and experimental results validate its performance over a misalignment range of $\pm 50\,\%$ of the transmission distance. Future work will involve fine-tuning the experimental system and exploring the impact on inverter performance.**

***Index Terms*—wireless power, capacitive power transfer, DC-DC conversion, misalignment**

I. Introduction

Near-field wireless power transfer is a key technology for a variety of applications, notably electric vehicle (EV) charging [1] and electrified roadways. While inductive power transfer is more established, resonant capacitive power transfer (RCPT) offers benefits like reduced metal heating, easier shielding, and cost-effectiveness [2]. However, achieving the power and efficiency required for EV charging at high switching frequencies, such as $13.56\,\mathrm{MHz}$, remains challenging. Differential RCPT systems, like those employing a six-plate structure, are particularly affected by lateral misalignment, giving rise to imbalances and common-mode (CM) currents [3]. This leads to increased reference and/or shield potentials and electromagnetic field emissions, thereby reducing safety and reliability while creating regulatory compliance challenges.

In RCPT implementations like the one described in [4], where the transmit resonator is driven by a quasi-constant current, imbalances caused by lateral misalignment are more pronounced in the receiver as it is effectively driven by a differential pair of quasi-constant voltage sources. These voltages are balanced under perfect alignment, but lateral misalignment introduces imbalances. When the outputs of the receiver's differential rectifier are tied together to feed a single-input single-output (SISO) DC-DC, the system is forced to operate at a single rectified voltage, giving rise to CM currents.

This paper proposes a dual-input single-output (DISO) DC-DC converter that presents independent and optimized load resistances to each rectifier output, suppressing CM currents and allowing the system to maintain safe and reliable RCPT operation under lateral misalignment. Additionally, measuring the DISO DC-DC's input voltages could enable dynamic misalignment correction, making it particularly suitable for applications like electrified roadways. While several converter topologies [5]–[10] and their control strategies [11]–[15] were explored, the proposed design is largely based on one presented in [5] due to its simple single-inductor design.

Section II introduces the RCPT system model and discusses rectifier loading under lateral misalignment. The proposed DISO DC-DC is detailed in section III. Simulations are detailed in section IV, followed by experimental validation in section V. Section VI concludes the paper.

II. RCPT System Model

The six-plate RCPT system under consideration is illustrated in Fig. 1. The transmit resonator is driven by a differential and load-independent inverter that behaves as a balanced quasi-constant current source via immittance conversion. Power is transferred wirelessly over a distance d, and the receiver can be laterally misaligned relative to the transmitter by x. Impedances Z_{tg} and Z_{rg} represent environmental or situational return paths and appear in parallel with those provided by plate self-capacitances. While the transmitter is assumed to be "grounded", i.e., Z_{tg} is small and inductive, the receiver is assumed "floating", i.e., Z_{rg} is large and capacitive. It is further assumed that the reference plane for the receive electronics is directly connected to the shield plate of the receive resonator, which exhibits a potential-to-ground of v_3. Thus, the differential and load-independent class-E synchronous rectifier (SR), described in [4] and outlined in red, is excited by $v_1 - v_3$ and $v_2 - v_3$. While other rectifier topologies could be used, such as class-D (active or passive), they would exhibit similar behaviour in this context.

The SR's input stage is a balanced double immittance converter composed of L_1, C_1, L_2, and C_2. Thus, $Z_{\mathrm{in1,2}} = Z_{\mathrm{rect1,2}}\left(C_2/C_1\right)^2$. Load-independent zero-voltage switching (ZVS) is ensured by L_{a}, L_{zvs}, and C_{zvs}. A series resonant filter

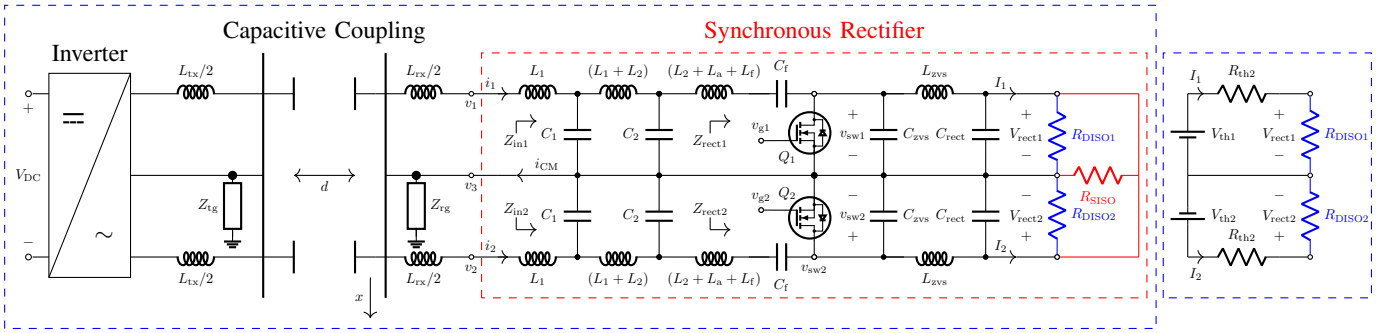

Fig. 1. Diagram illustrating the RCPT system under consideration. Right: Equivalent Thevenin model when the DISO DC-DC suppresses CM current.

consisting of L_f and C_f ensures the input current is sinusoidal, while C_{rect} minimizes output voltage ripple.

When the SR drives a SISO DC-DC (the red loading configuration in Fig. 1), $V_{rect1} = V_{rect2}$, and this common voltage drives the input resistance of the DC-DC, denoted by R_{SISO}, resulting in substantial CM current under lateral misalignment. Alternatively, the proposed DISO DC-DC allows each rectifier output to be loaded independently, i.e., V_{rect1} and V_{rect2} drive R_{DISO1} and R_{DISO2}, respectively (the blue loading configuration in Fig. 1). By setting R_{DISO1} and R_{DISO2} to achieve the desired output power while ensuring $I_1 = I_2$, i.e., $i_1 = -i_2$, CM current can be suppressed. When this is the case, a Thevenin model of the SR output can be defined as shown on the right side of Fig. 1. This will be used to design the DISO DC-DC.

Power-sharing between the receive branches, e.g., the percentage of total load power delivered by each branch, should be monitored. While both would deliver $50\,\%$ when $x = 0$, unequal load sharing is expected under misalignment, requiring some de-rating of the system's power capacity.

III. Design of the Proposed DISO DC-DC

A schematic for the proposed DISO DC-DC is shown in Fig. 2. It is modified from [5], as it is operated synchronously to maximize efficiency and alternately engages two sets of high-side bidirectional switches, (Q_1 + Q_2 and Q_4 + Q_5) to prevent reverse currents when the rectified voltages differ. The converter has four sequential operating modes shown in Table I, where T and t_0 are the cycle period and start time, respectively. The switching duty cycles for each branch, D_1 and D_2, operate $180°$ out of phase. Note that the common ground symbol used here is equivalent to node v_3 in Fig. 1.

TABLE I
Switching Operation of the Proposed DISO DC-DC.

Mode	Activated Switch	Switch Timing
Mode 1	Q_1, Q_2	$t_0 \rightarrow D_1(T/2)$
Mode 2	Q_3	$D_1(T/2) \rightarrow T/2$
Mode 3	Q_4, Q_5	$T/2 \rightarrow (1-D_2)\,(T/2)$
Mode 4	Q_3	$(1-D_2)\,(T/2) \rightarrow T$

The relationship between D_1, D_2, and the output voltage, V_o, was derived assuming ideal switches, lossless inductors and capacitors, L is large enough that its current is relatively

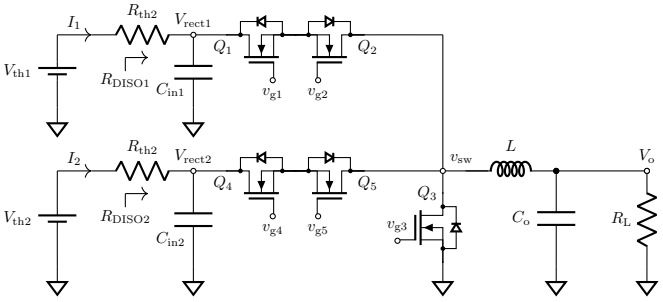

Fig. 2. Proposed DISO DC-DC schematic.

constant and equal to the load current, and C_{in1} and C_{in2} are large enough to keep the currents through R_{th1} and R_{th1} relatively constant. Thus, the current into each converter branch is given by the average of a square wave with a peak equal to the load current and timings based on the corresponding duty cycle. Setting $D_1 = D_2 = D$ ensures $I_1 = I_2$, effectively suppressing CM current. In this case,

$$V_o = \frac{2R_L D\,(V_{th1} + V_{th2})}{D^2\,(R_{th1} + R_{th2}) + \dfrac{4R_L}{\eta_{DISO}}}, \tag{1}$$

where η_{DISO} is the efficiency of the DISO DC-DC. Also,

$$D = \frac{2R_L V_{th1}}{V_o\,(R_{DISO1} + R_{th1})} = \frac{2R_L V_{th2}}{V_o\,(R_{DISO2} + R_{th2})}. \tag{2}$$

IV. Simulations

The six-plate structure described in [3] was modelled in CST Studio Suite. The nominal transmission distance is $d = 120\,\text{mm}$, which translates to a coupling coefficient of $k_e = 0.09$. Simulated capacitance matrices were produced over a lateral misalignment range of $-60\,\text{mm} \le x \le 60\,\text{mm}$, or $\pm 50\,\%$ of d, in $10\,\text{mm}$ steps. These capacitances were used to define an equivalent circuit model of the capacitive interface in LTspice® for a given misalignment condition. Split-L resonating inductors were added such that the unloaded quality factor of the resonators was approximately 450. The transmit resonator was driven at $13.56\,\text{MHz}$ by a differential pair of $2\,\text{A(RMS)}$ current sources with $5\,\text{k}\Omega$ source resistances, which serve as a model for the inverter. This

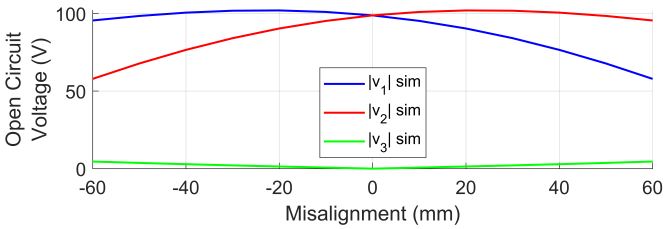

Fig. 3. Simulated RMS open-circuit voltage magnitudes of the resonator outputs under lateral misalignment.

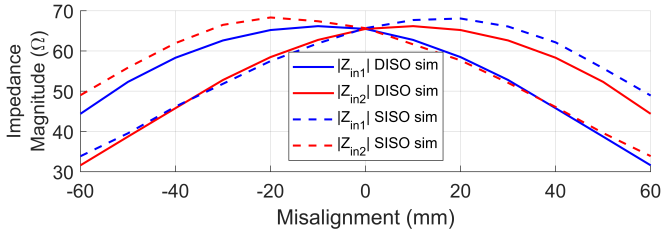

Fig. 5. Magnitude of the impedance presented by the SR

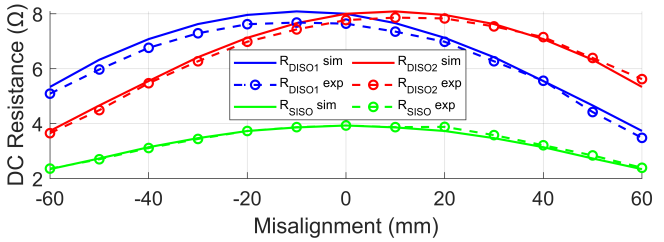

Fig. 4. DC resistances presented by both SISO and DISO DC-DCs under lateral misalignment.

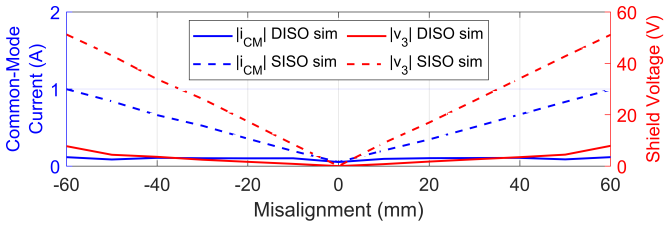

Fig. 6. Simulated RMS CM current and worst-case RMS shield voltage under lateral misalignment for both DISO and SISO configurations.

simulation yielded the open-circuit values for v_1, v_2, and v_3 under lateral misalignment shown in Fig. 3. While v_1 and v_2 are complementary, v_3 is symmetrical and gradually increases with lateral misalignment.

Next, the receive resonator was terminated in a model of the SR from [4], which was tuned to ensure load-independent ZVS with a nominal rectified voltage of approximately 32 V under perfect alignment. Referring to Fig. 1, the red output connections simulate loading by a SISO DC-DC, and R_{SISO} was varied to maintain the desired output power of 250 W with an additional 5 W to compensate for a 98 % efficient DC-DC at each value of x. The blue output connections model loading by the proposed DISO DC-DC, where the added constraint of $I_1 = I_2$ allows proper selection of R_{DISO1} and R_{DISO2}. These output resistances are plotted in Fig. 4 along with their experimental values, while the corresponding impedances presented to the receive resonator are shown in Fig. 5. Note that the impedances presented by DISO loading tend to follow the corresponding open-circuit voltages under misalignment, thus maintaining equal currents, while SISO loading does the opposite. This is reflected in Fig. 6, which clearly shows that the CM current increases linearly with lateral misalignment under SISO loading, whereas it is minimized under DISO loading.

The impact of CM current on v_3 depends on Z_{rg}. For a "floating" receiver, Z_{rg} will be large and capacitive. As it appears in parallel with the return paths offered by plate self-capacitances, the worst-case v_3 will be observed for a given CM current as $|Z_{\mathrm{rg}}| \to \infty$. These worst-case shield potentials are also shown in Fig. 6 for both SISO and DISO loads. In addition to exacerbating electromagnetic compatibility (EMC) challenges, the CM current produced for SISO loads can cause the shield plate to reach hazardous touch potentials.

In terms of power sharing, SISO and DISO loading led to one branch supplying up to 60.1 % and 58.7 % of the load at ±60 mm, respectively. Thus, system power capacity should be de-rated by approximately 16.8 % to accommodate this much lateral misalignment.

An LTspice® simulation was conducted for the DISO DC-DC, using the equivalent Thevenin output of the SR as its input. The converter produces an output voltage of 20 V, which translates to a load resistance, R_{L}, of 1.6 Ω at the desired output power of 250 W. A switching frequency of 200 kHz was chosen as a compromise between component size, complexity, and emissions. The ISZ0702NLSATMA1 MOSFET was used for all switching components. The VER2923-153KL 15 µH inductor was chosen to set the converter in continuous conduction mode and ensure a simulated current ripple of less than 10 %. To keep the simulated output voltage ripple below 0.02 %, two parallel EEHZA1H680P 68 µF capacitors were used for Co. The PMEG050T150EPDZ diode was placed in parallel with Q_3 to reduce switching stresses. The value of D required to maintain $I_1 = I_2$ and $V_{\mathrm{o}} = 20$ V ranges from 65 % when $x = 0$ to 87 % at $x = \pm$ 60 mm. The resulting converter efficiency, η_{DISO}, was found to be a nearly constant 98 %. The experimental efficiency is expected to be lower due to trace resistances and auxiliary gate drive circuitry.

V. Experimental Implementation

The proposed DISO DC-DC was implemented experimentally. It includes 12 V and 3.3 V auxiliary supplies, input and output voltage and current sensing, gate driving circuits, heat sinks, and a dsPIC33EP microcontroller for the generation of PWM signals and output voltage regulation, which achieved by a proportional-integral (PI) control method.

Fig. 7 shows the full 13.56 MHz RCPT system, with the proposed DISO DC-DC highlighted in the top right corner. Note that the SR is obscured by the shield of the receive

resonator. An existing SISO DC-DC was used as baseline, which provides a regulated output of 30 V using the LT8392 as its buck-boost DC-DC controller.

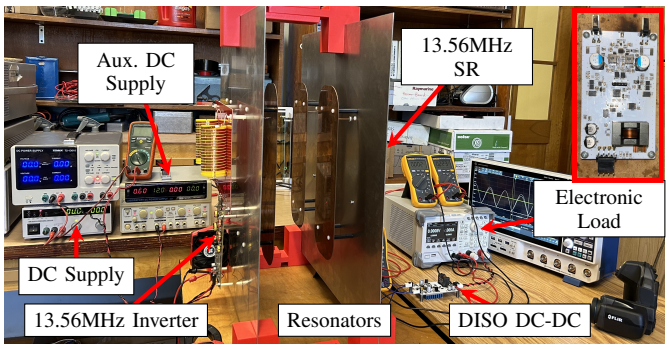

Fig. 7. Experimental set-up of the RCPT system with inset image of the DISO DC-DC

As the CM current within the SR is difficult to measure, the DC output currents of each rectifier branch were used to provide a measure of CM current reduction. The resonators were misaligned in increments of 10 mm from −60 mm to 60 mm. At each misalignment, the load was increased from no load to 250 W in steps of 50 W. Fig. 8 shows the measured end-to-end efficiency results over the full load range for both DISO and SISO loading at $x = 0$ and ±60 mm. End-to-end efficiency is relatively insensitive to both lateral misalignment and SISO versus DISO loading. The experimental DISO DC-DC achieved ≈96.0 % efficiency under misalignment, while the SISO DC-DC efficiency was ≈96.9 %.

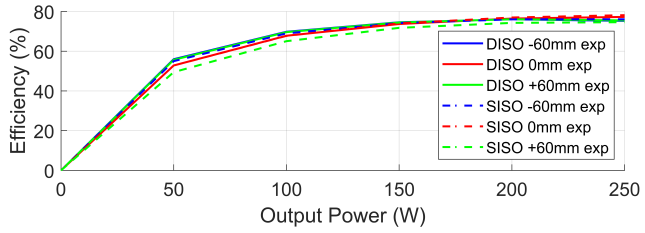

Fig. 8. End-to-end efficiency of the system including SISO or DISO DC-DC

Fig. 9 shows the full-load rectifier output currents (I_1 and I_2). The DISO results agree well with simulation, exhibiting a maximum error of 4.1 %. Though the measured and simulated SISO results are qualitatively similar, the maximum error is much higher at 17.7 %. This likely stems from tuning imperfections in the RCPT link and SR, as well as the finite value of Z_{rg}, which the system is more sensitive to in the presence of CM current. Regardless, it is clear that the proposed DISO DC-DC is effectively maintaining $I_1 \approx I_2$ (I_1 is slightly higher as it supplies the DISO's auxiliary circuitry), thereby suppressing CM current and reducing the receive-side shield potential, whereas the SISO DC-DC does not.

In terms of power-sharing, one branch provided 54.2 % and 58.8 % for the SISO and DISO, respectively, at −60 mm. At 60 mm, the other branch provided 62.03 % and 61.38 % for the SISO and DISO, respectively. The differences at ±60 mm

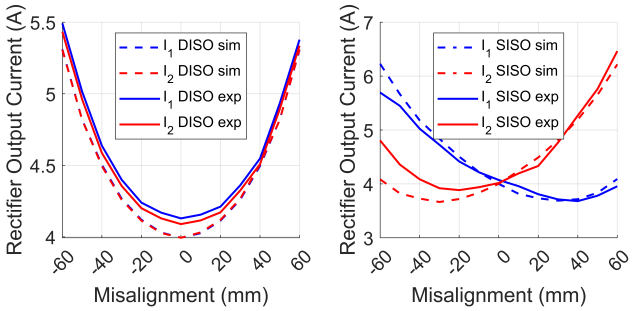

Fig. 9. SR output currents at full load for both loading types.

are likely due to tuning imperfections. However, the power-sharing results tend to agree well with simulation on average.

VI. Conclusion

Relative to a conventional SISO DC-DC, the proposed DISO DC-DC significantly reduces CM currents in RCPT systems under lateral misalignment, effectively lowering shield voltages and mitigating electromagnetic emissions. This is expected to improve the safety, reliability, and EMC performance of the technology, without significantly impacting power sharing and efficiency. Future work will concentrate on refining the tuning of the experimental system and examining how these different loading types affect the transmit side.

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