A Programmatic Method For Selecting Transistors For High-Frequency Class-E Amplifiers

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***Abstract*—Radiative wireless power transfer at high efficiency can be achieved with Class-D or Class-E amplifiers. These amplifiers have achievable efficiencies that can be very high but heavily depend on transistor selection. The objective of this work was to partially automate the selection process to quickly generate near-optimal Class-E amplifier designs entirely within MATLAB®. The candidate transistor SPICE models were parsed and converted into a system of first-order ordinary differential equations. A non-stiff numerical solver was used to find steady-state solutions for candidate circuits. A simplex search algorithm was used to find the maximum-efficiency candidate circuit for the transistor. The results were also simulated in LTspice® to confirm accuracy. Eighty-four transistors were compared and seven were found to have high efficiency capabilities at 2.45 GHz. The best performing device achieved 60.6% power-added efficiency in MATLAB®, and the same device achieved 53.0% power-added efficiency in LTSpice®. The incongruency between this work and LTSpice® was small enough to justify its use for eliminating large numbers of candidate transistors.**

Keywords—Radiofrequency amplifiers, power amplifiers, circuit optimization, wireless power transmission, switching circuits

I. Introduction

RF amplifiers for wireless power transfer (WPT) and communication systems are used to produce sinusoidal signals efficiently. The motivation for operating efficiently is that power lost by the amplifier is mostly converted into heat. This heat can limit the power handling capability of the amplifier, induce failure of the circuit, and wastes energy that could otherwise have been used elsewhere. For terrestrial power and communications infrastructure, efficiency is less critical because the atmosphere can be used for cooling and fixed transmitter platforms can make use of grid power. In contrast, amplifier losses are significant for nanosatellite communication systems because the thermal management system is limited to radiative cooling and wasted power reduces the energy available to perform other tasks [1].

Traditional non-switching amplifier topologies like Class-A have theoretical peak efficiencies as low as 50%. Switching amplifier topologies like Class-D and Class-E are attractive because their theoretical efficiency is 100% [2]. Class-D amplifiers often lose this efficiency at higher operating frequencies because the dead-time insertion becomes a significant part of the operating cycle. The challenges of driving the high-side transistor often reduce the maximum operating frequency below those used for communication and far-field WPT systems. Class-E amplifiers eliminate both considerations by using a single low-side transistor [3]. The main drawbacks of this topology are the voltage and current stresses placed on the transistor, which are much higher than those of a Class-D amplifier, resulting in a lower power handling capacity for a given transistor. Because we aim to operate at low power, Class-E can be used effectively in the S-band.

Traditional Class-E amplifier design can be performed analytically; however, once the on-resistance of the transistor is considered, there is no analytical method for finding an optimum design [4, 5], necessitating the use of numerical computation. Existing methods typically involve manual adjustment of circuit parameters and simulation with various SPICE programs. Optimizing the design requires on the order of 300 iterations [4], and manual intervention requires an experienced designer. One proposed method involves using multiple tools, one for simulation and one for optimization [6]; however, the invocation of simulation tools by an optimization tool often increases the time required to solve the circuit when compared to simulation tools built into the optimization tool.

This paper introduces a method for performing design optimization of Class-E amplifiers for radiative WPT or wireless communication systems in minutes without the intervention of SPICE simulators. Instead, MATLAB® is used to perform simulation and design optimization for over 100 transistors.

Section II details the topology of the model used, while section III described the selection of optimization goals and initial conditions. Section IV presents the simulation results, and section V offers concluding remarks and directions for future work.

II. Circuit Modelling

The parasitic capacitances, inductances, and resistances of the transistor are important sources of loss in high-frequency Class-E amplifiers. This is often modeled as a capacitive loop between the internal drain, source, and gate nodes, with resistive and inductive elements connecting those internal nodes to the pads of the device. The inductances introduced by the transistor itself are usually insignificant compared to the layout loop inductances, so they are rarely included in the transistor model. The circuit model in Fig. 1 shows these transistor parasitics within the dashed box.

The lumped-element approximation of a FET is often used to model the operation of the transistor in SPICE. This research considers a SPICE library provided by Efficient Power Conversion Corporation (EPC). All FET models in this library are structured identically. Because of the consistent structuring of these SPICE models, programmatically parsing the library to extract transistor parameters and behavioural equations is trivial. While the overall approach is not limited to this SPICE library, the specific text parsing element is.

MATLAB® is capable of numerically iterating systems of ordinary differential equations (ODEs) if they are expressed as a system of first-order ODEs. The SPICE netlist that describes the circuit cannot be simulated directly. Instead, leveraging the identical structure of Class-E amplifiers and transistor parasitics allows the system to be manually converted to a set of ODEs, which can then be simulated.

The overall circuit to be simulated, shown in Fig. 1, consists of four capacitors, of which three have voltage dependence, two inductors, four resistors, one voltage-controlled current source, and two voltage sources. To express this circuit as a system of first-order ODEs, each reactive element must have their state variable derivatives expressed in terms of boundary conditions (voltage sources) and other state variables.

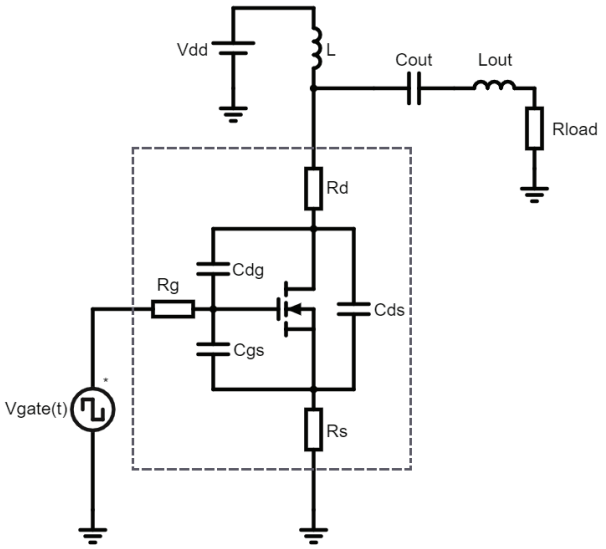

Fig. 1. A traditional Class-E amplifier which relies on the intrinsic capacitance of the switching device. The dashed box contains the lumped-element model of the transistor.

One challenge that arises is the loop of parasitic capacitors inside the FET. The voltage across C_{ds} must be the sum of the voltage across C_{gs} and C_{dg} shown in (1). Taking the derivative of this results in the additional equality in (2) that balances the current around the loop. Rearranging these expressions allows instances of V_{cdg}, shown in (3), and I_{cdg}, shown in (4), to be expressed solely in terms of the voltage across and current through C_{gs} and C_{ds}, respectively,

$$V_{Cds} = V_{Cgs} + V_{Cdg} \tag{1}$$

$$I_{Cds}/C_{ds} = I_{Cgs}/C_{gs} + I_{Cdg}/C_{dg} \tag{2}$$

$$V_{Cdg} = V_{Cds} - V_{Cgs} \tag{3}$$

$$I_{Cdg} = C_{dg}\left(I_{Cds}/C_{ds} - I_{Cgs}/C_{gs}\right). \tag{4}$$

Consequently, the drain-gate capacitor can be replaced with a current-controlled current source. The voltage loops through the rest of the circuit are summarized by (5), (6), and (7),

$$V_{Rload} + V_{Cout} + V_{Lout} + V_L - V_{DD} = 0 \tag{5}$$

$$V_{Rs} + V_{Cds} + V_{Rd} + V_L = 0 \tag{6}$$

$$V_{Rs} + V_{Cgs} + V_{Rg} - V_{gate} = 0. \tag{7}$$

The current through R_{load} is denoted by I_{load}, the current from V_{dd} is denoted by I_{feed}, and the current through the transistor itself is denoted by I_{ds}. The currents branching through the switching node, internal drain node, internal gate node, and internal source node are in (8), (9), (10), and (11), respectively,

$$I_{feed} = I_{load} + I_{Rd} \tag{8}$$

$$I_{Rd} = I_{Cds} + I_{Cdg} + I_{ds}\left(V_{Cds}, V_{Cgs}\right) \tag{9}$$

$$I_{Cdg} = I_{Cgs} + I_{gate} \tag{10}$$

$$I_{Cgs} + I_{ds}\left(V_{Cds}, V_{Cgs}\right) + I_{Cds} = I_{Rs}. \tag{11}$$

The system of five ODEs required to simulate the circuit are described by (12), (13), (14), (15), and (16),

$$I'_{Rload} = V_{Lout}/L_{out} \tag{12}$$

$$V'_{Cout} = I_{Rload}/C_{out} \tag{13}$$

$$I'_{feed} = V_{Lout}/L_{feed} \tag{14}$$

$$V'_{Cds} = I_{Cds}/C_{ds} \tag{15}$$

$$V'_{Cgs} = I_{Cgs}/C_{gs}. \tag{16}$$

Substituting and rearranging the first 11 equations into the system of ODEs to eliminate non state variables yields the following complete set of expressions in (17) through (21), which were used to simulate the complete circuit,

$$\begin{aligned} I'_{out} = \Big(V_{Cds} - V_{Cout} + R_d\left(I_{feed} - I_{out}\right) - I_{out}R_{out} \\ - R_s\left(V_{Cgs} - V_{gate} - I_{feed}R_g \right. \\ \left. + I_L R_g\right)/\left(R_g + R_s\right)\Big)/L_{out} \end{aligned} \tag{17}$$

$$V'_{Cout} = I_L/C_{out} \tag{18}$$

$$\begin{aligned} I'_{feed} = (V_{dd} - V_{Cds} - R_d\left(I_{feed} - I_{Rload}\right) + R_s(V_{Cgs} \\ - V_{gate} - I_{feed}R_g \\ + I_{Rload}R_g)/(R_g + R_s)))/L_{feed} \end{aligned} \tag{19}$$

$$\begin{aligned} V'_{Cds} = (\frac{V_{gate} - V_{Cgs} + R_g\left(I_{feed} - I_{Rload}\right)}{R_g + R_s} \\ - I_{ds}\left(V_{Cds}, V_{Cgs}\right))/C_{ds} \end{aligned} \tag{20}$$

$$\begin{aligned} V'_{Cgs} = (-\frac{C_{gs}\left(V_{Cgs} - V_{gate} + I_{feed}R_s - I_{Rload}R_s\right)}{C_{dg}\left(R_g + R_s\right)} \\ - (C_{gs}\left(V_{Cgs} - V_{gate}\right. \\ + R_g I_{ds}\left(V_{Cds}, V_{Cgs}\right) \\ + R_s I_{ds}\left(V_{Cds}, V_{Cgs}\right) - I_{feed}R_g \\ \left. + I_{Rload}R_g\right))/(C_{ds}\left(R_g + R_s\right))) \\ /C_{gs}. \end{aligned} \tag{21}$$

III. Optimization Objective and Initial Conditions

The simulator runs until the state variables at the end of a cycle are nearly equal to those at the beginning of the cycle. A scalar value describing circuit operating point informs the optimizer, *fminsearch*, whether the change in circuit parameters was effective or not. The simplest objective function is to subtract the system's total efficiency from 1, shown in (22),

$$F_{obj}(x) = 1 - \frac{1}{T}\int ({I_{Rload}}^2 R_{load}/({I_{Rload}}^2 R_{Rload} + I_{feed}V_{dd} + I_{gate}V_{gate}))dt. \quad (22)$$

This objective function has two major failings. First, the output power is evaluated across the entire frequency spectrum instead of at the fundamental frequency. This means that energy lost in output harmonics are being treated as contributors to the useful output power. Considering the goal of the amplifier is to produce a pure sinusoid, the numerator should be replaced with the Fourier series of the load current, shown in (23),

$$F_{obj}(x) = 1 - \frac{1}{T}\int ({I_{Rload,fund}}^2 R_{load} /({I_{Rload}}^2 R_{Rload} + I_{feed}V_{dd} + I_{gate}V_{gate}))dt. \quad (23)$$

Second, the objective function does not consider whether the system's operating point will damage the transistor. The operating limits can be implemented as a conditional multiplier. If the limits of the transistor are exceeded, η is multiplied by 0.1. It is important to avoid selecting a multiplier that is too small, because it will prevent the optimizer from temporarily exceeding the operating limits to find a better solution.

To encourage more realistic inductor value selections, additional losses were added to the denominator of the efficiency evaluation assuming an unloaded Q factor of 100.

The generalized design equations in [7] were used to generate strong initial solutions to be optimized. This is important because the optimizer is local and requires a starting condition which is already close to the optimal solution.

IV. Results

All transistors in the EPC Co. GaN FET library were parsed into MATLAB® compatible equations and substituted into the system of equations from (21) to (25). Of the 108 devices, only 82 of them are single, independent transistors that are useful for Class-E amplifiers. The operating frequency selected for evaluation was the 2.45 GHz because it is the center of the 2.4 GHz ISM band. Fig. 3 shows that a subset of those 82 transistors are capable of high-efficiency operation, defined as > 50% power-added efficiency, at the selected frequency.

In the high-efficiency region of interest, it is found that the achievable operating efficiency is inversely related to gate-source capacitance. As Fig. 2 illustrates, the most efficient selections have a high gate cut-off frequency. The gate switching time is limited by the RC low-pass network consisting of R_g, R_s, and C_{gs}. The operating frequency of the circuit is indicated by a vertical orange line. As the gate-source capacitance increases, the power consumed in driving the gate becomes a significant portion of the overall power lost. Devices with larger gate-source capacitance without a corresponding reduction of gate and source resistances limit the achievable operating frequency. Consequently, some devices with low gate cut-off frequencies do not achieve steady state during the operating cycle.

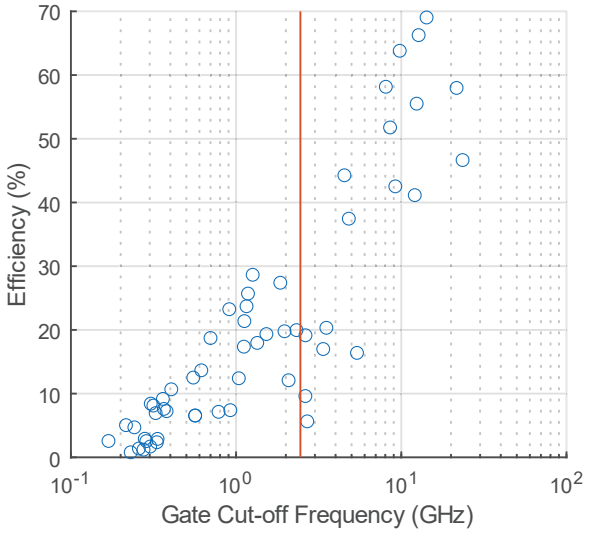

Fig. 2. Efficiency plotted against gate drive cutoff frequency. A preference for low capacitance at high frequencies is shown. The vertical orange line indicates a cutoff of 2.45 GHz. High efficiency can only be achieved well to the right of the line.

At the chosen operating frequency, it may appear that increasing the gate cut-off frequency generally yields higher efficiency. Fig. 3 shows that cut-off frequency is positively correlated with the drain-source resistance. Thus, it may appear that increasing the drain-source resistance generally improves efficiency; however, it is important to note that the power lost in conduction through the switch will eventually overcome the power saved by reducing the length of the transient period, resulting in a net decrease in efficiency.

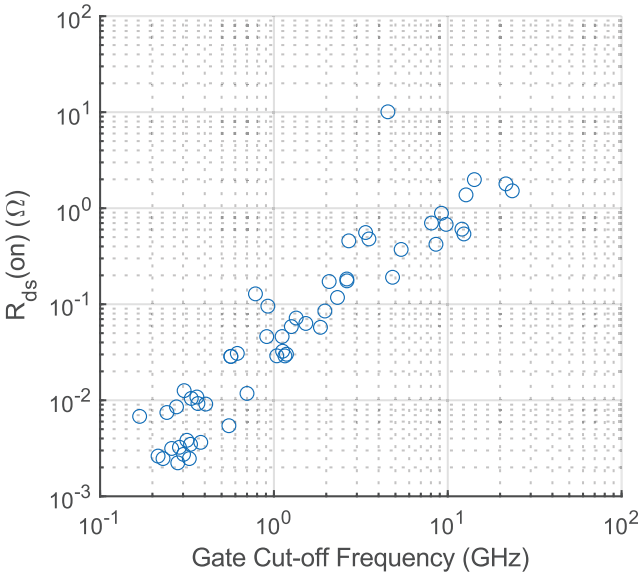

Fig. 3. Drain-source on resistance plotted against gate drive cutoff frequency. Transistors exhibiting faster switching times also exhibit higher conduction losses.

There also exists a close, linear relationship between gate-source and drain-source capacitance of the candidate set of transistors because they are all produced with similar materials and transistor geometries. This is illustrated in Fig. 4 and could be used to extrapolate the properties of the ideal transistor for a given operating regime using the same process without the use of more in-depth analysis methods.

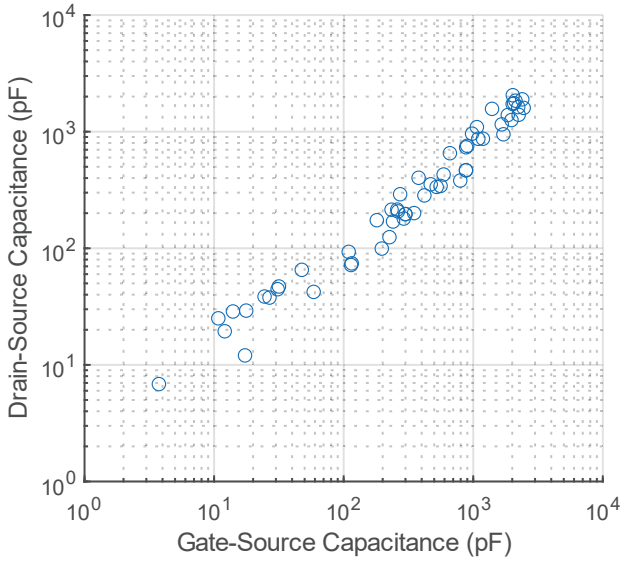

Fig. 4. Drain-source capacitance plotted against gate-source capacitance. The properties of the transistors in the library utilized are mostly similar.

The optimizer was given many degrees of freedom in the design. The gate drive waveform was assumed to be rectangular, but the on and off voltages and duty cycle were allowed to vary. For devices with sufficiently low gate cut-off frequency, the gate drive voltages can be reduced to bring the MOSFET closer to the threshold voltage. This increases the drain-source on resistance, but results in reduced gate drive losses, balancing the two sources of transistor loss.

The ratio of the resonant frequency of the feed inductor and drain-source capacitor compared to the switching frequency, denoted by q in [7] and [8], is an important figure for maintaining load independence in Class-E amplifiers for WPT applications. While load-independence was not a goal given to the optimizer, this work and [7] show that the peak efficiency condition often occurs in when DC feed inductance is finite and near that of a load-independent system. For example, the q value was 1.43 for the highest efficiency solution. This is evident because of the large AC component of the feed inductor current in Fig. 5.

It is important to note that the results shown in Fig. 2 were obtained without constraining the output power, i.e., they each settled on the power level that yielded the best performance. To facilitate comparisons with LTspice® simulations, the output power will be constrained to 2 W for the remainder of the paper. From the 82 transistors, the best performing device was the EPC8008. It achieved an overall efficiency of 60.6%. The same circuit was simulated in LTspice® using the same SPICE model, yielding an efficiency of 53.0%. Fig. 5 shows the operating waveforms of this circuit in MATLAB®, LTspice® without further optimization, and in LTspice® after optimization, while Table 1 summarizes the corresponding circuit parameters. The difference between results is likely caused by the different solver methods used between simulation programs. In MATLAB® a Runge-Kutta solver is used, whereas LTspice® uses the default built-in solver. The solver error tolerances were left at their default settings and the minimum timestep was chosen to ensure a minimum of 100 steps per period. While there is a difference in the results provided by the simulator, the MATLAB® solution simulates an iteration in 0.08 seconds, while the LTspice® iteration time is 1.8 seconds. Thus, the potential loss of accuracy is balanced by the large increase in simulations per second.

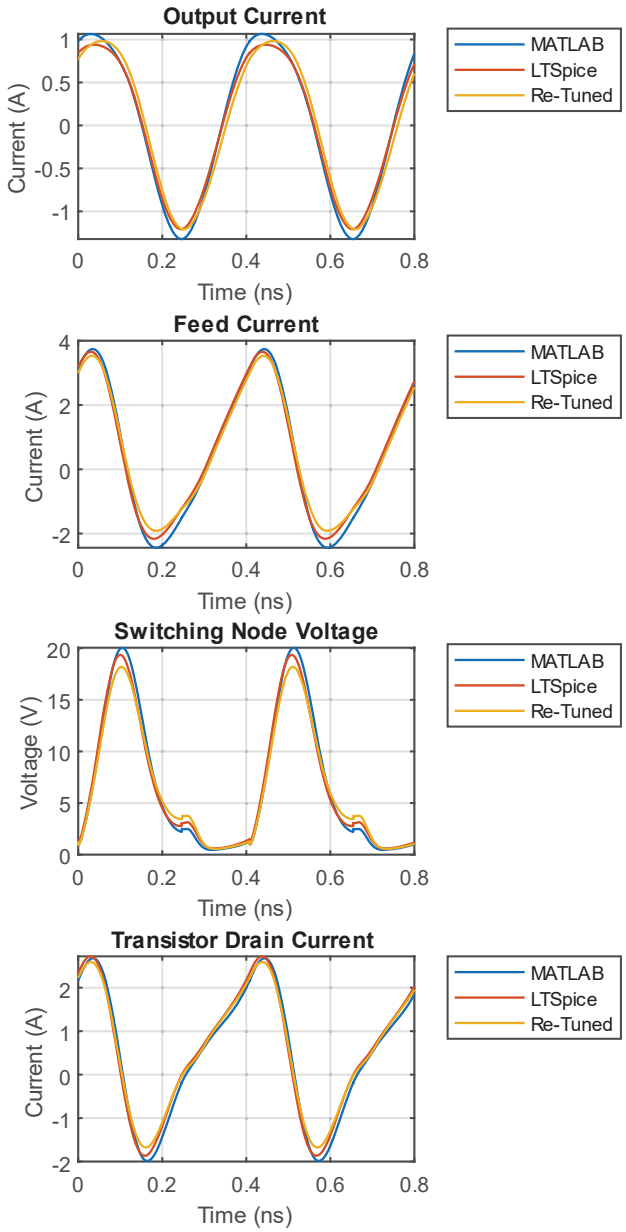

Fig. 5. Operating waveforms of the achieved EPC8008 Class-E amplifier design. Blue is the result generated by MATLAB®, red is the result generated by LTSpice® without modification, and yellow is the further tuned result generated by LTSpice®.

Table 1 – Circuit parameters for ideal 2 W output power solution achieved with MATLAB® and LTspice®.

	MATLAB®	LTspice®
L (nH)	0.193	0.192
L_{out} (nH)	1.34	1.35
C_{out} (pF)	2.40	2.45
V_{DD} (V)	6.615	6.490
V_{gate_off} (V)	0.014	0.014
V_{gate_on} (V)	2.787	2.842
D (%)	39.6	39.4
R (Ω)	3.274	3.257

Comparing the efficiency to that achieved by Kobayashi [9], this work yields only 2.7% less power-added efficiency at the maximum efficiency operating point.

V. Conclusion and Future Work

The proposed method of semi-automated circuit simulation and optimization allows a designer to easily compare the potential performance of many candidate transistors in a short period of time. The results and [7] indicate that a finite DC feed inductance permits the achievable efficiency to increase. While the method is capable of accommodating circuits of any complexity, additional elements like load matching networks and loop inductance can increase the number of ODEs simulated from 5 to over 10, resulting in much slower iterations. Considering that over 1000 iterations are required for every transistor, it is of interest to eliminate poorly performing transistors before increasing system complexity and simulation fidelity.

While the circuits simulated have been created using lumped elements, the impact of a manufacturable layout of components, potentially replacing lumped elements with transmission-line stub equivalents, should be explored. Additionally, further constraining the optimization to prioritize tuning insensitivity would aid in producing manufacturable designs without being impacted by the specifics of circuit layout. Furthermore, the gate drive waveform could be something other than a rectangular wave, potentially allowing the circuit to operate with lower gate-drive losses for the same drain loss performance.

Acknowledgment

This work would not have been possible without the funding provided by the New Brunswick Innovation Foundation (NBIF) and the University of New Brunswick (UNB).

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