

Development of Passive Anti-Islanding Strategies for Distributed Generation Systems

by

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Abstract

Detecting and removing islanding operation are necessary for the large-scale deployment of distributed generators (DGs) in electric power systems (EPS), as mandated by different standards and industrial practices. Although passive islanding detection techniques have no impact on EPS functions, they possess a shortcoming characterized by a large non-detection zone (NDZ) over which islanding detection may fail, resulting in unsafe operation and non-compliance with the interconnection standards.

New anti-islanding detection and protection methods are developed and presented in this dissertation, which focus on the operating space where existing methods fail. The developed techniques aim to realize reliable and timely islanding detection over all operating conditions. The frequency dependent impedance (FDI) concept is presented as a means of islanding detection that is based on spectral decomposition of voltage and current at the point of common coupling (PCC). The impedance frequency technique (ZFT) concept is presented as a new anti-islanding algorithm. In addition, a passive anti-islanding algorithm, which is independent from the power electronic converter (PEC) and is based on the virtual power signal (VPS) with improved anti-islanding performance, is introduced and tested online. Furthermore, the zero sequence impedance (ZSI) concept is a new passive anti-islanding algorithm that is developed employing the wavelet packet transforms (WPT). The ZSI algorithm is reliable and timely for detecting the islanding operation, and may be applied for DG systems with PECs and DG systems without PECs.

The developed methodologies are explored analytically, validated in simulation,

and tested experimentally. Performance results demonstrate the effectiveness of the proposed anti-islanding methods in comparison with existing methods.

To My Parents

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Table of Contents

Abstract	ii
Dedication	iv
Acknowledgments	v
Table of Contents	vii
List of Tables	xi
List of Figures	xii
Abbreviations	xvi
1 Introduction	1
1.1 Problem Overview	3
1.2 Literature Survey	5
1.2.1 Active Anti-islanding Methods	8
1.2.1.1 Impedance Technique	9
1.2.2 Passive Anti-islanding Methods	9
1.2.2.1 UV/OV and UF/OF	10
1.2.2.2 Rate of Change of Active Power	11
1.2.2.3 Rate of Change of Frequency	12

1.2.2.4	Phase Jump Detection	12
1.2.2.5	Voltage and Current Harmonics	12
1.2.2.6	Non-Detection Zone Characterization	13
1.3	Research Objective	14
1.4	Research Methodology	15
1.5	Summary of Research Contributions	18
1.6	Dissertation Outline	19
2	A Frequency Dependent Model	21
2.1	Introduction	21
2.2	System Description	21
2.2.1	Hypothesis	23
2.3	Simple Harmonic Model Type-I	24
2.4	PEC-Interfaced DG Systems	25
2.4.1	Simple Harmonic Model Type-II	28
2.4.2	Simple Harmonic Model Type-III	30
2.5	Assumptions for Analysis and Parameters	31
2.6	Analysis Results	32
2.7	Impedance Based on Measurements of Voltage and Current	35
2.7.1	Approach Overview	36
2.8	Summary	37
3	Simulation and Experimental Tests	40
3.1	Introduction	40
3.2	System Configurations	41
3.2.1	Simulation Model	41
3.2.2	Experimental Test bed	42
3.2.3	Analytical Model	43

3.3	Impedance-Based Analysis	44
3.3.1	Impedance Based Network Topology (ZTF)	46
3.3.2	Grid Impedance Estimation	47
3.3.3	Impedance Based on FFT Technique (ZFT)	48
3.3.4	Fitting Impedance Measurements to Transfer Function Model (ZLS)	49
3.4	Implementing the ZFT Based Anti-islanding Method	52
3.5	Results and Discussion	53
3.6	Specifying the Non Detection Zone (NDZ)	60
3.7	Performance Comparison	61
3.8	Summary	61
4	Online Testing of VPS Index	64
4.1	Introduction	64
4.2	The VPS Based Algorithm	65
4.3	Development of Hardware Platform	69
4.4	Systems Configurations	70
4.4.1	Simulation System	70
4.4.2	Experimental Test Systems	73
4.5	Simulation and Experimental validation	75
4.5.1	Simulation validation	75
4.5.2	Experimental validation	75
4.5.3	Detection Time	79
4.6	Discussion	80
4.7	Summary	81
5	Time Frequency Dependent Based Index	82
5.1	Introduction	82

5.2	System Test Configurations	83
5.2.1	Simulation Model	83
5.2.2	Experimental Setup	84
5.3	Symmetrical Component and WPT	85
5.4	Feature Extraction	87
5.5	Anti-islanding Algorithm	90
5.6	Evaluation Criteria	91
5.7	Simulation Tests and Discussion	92
5.8	Experimental Tests and Discussion	96
5.9	Summary	98
6	Conclusions	100
6.1	Summary	100
6.1.1	Overview of Contributions	102
6.2	Recommendations for Future Work	103
6.3	Final Comments	104
	Bibliography	105
	Appendices	115
A	Appendixes	115
A.1	Inverter Control Scheme	115
A.2	Mathematical Exploration for System Identification	117
	Vita	

List of Tables

2.1	System Parameters	32
2.2	Grid Impedance Parameters	32
3.1	System Parameters	44
4.1	Simulation System Parameters	71
4.2	Experimental System Parameters	74
A.1	Inverter Model I12-60 Specified Parameters	116
A.2	Simulation System Parameters for PEC Based System and no PEC Based System	122

List of Figures

1.1	A DG interconnection with the EPS.	2
1.2	Islanding detection challenges.	4
1.3	Classification of anti-islanding methods.	6
1.4	A structure for the frame work of the proposed anti-islanding methods.	15
2.1	Harmonic model of DG-EPS system without PEC.	22
2.2	Transfer function model of grid-DG system.	23
2.3	Harmonic model of the DG-EPS system with EPC.	26
2.4	Inverter control diagram with EPS input.	26
2.5	Feedback control diagram of the inverter based DG-EPS system.	27
2.6	Feed-froward control diagram of the inverter based DG-EPS system.	28
2.7	Bode of $ Z_{PCC} $ for Model-I in normal and islanding operation.	33
2.8	Bode of $ Z_{PCC} $ for Model-II in normal and islanding operation.	33
2.9	Bode of $ Z_{PCC} $ for Model-III in normal and islanding operation.	34
2.10	Anti-islanding flowchart.	38
3.1	A schematic diagram of simulation system.	41
3.2	A schematic diagram of the experimental test bed.	42
3.3	A photo of the experimental setup for 10 kW DG.	43
3.4	A schematic diagram of the simplified electric circuit topology.	44

3.5	Flow diagram depicting the passive anti-islanding algorithm for the objective function.	54
3.6	Superimposed of the load impedance, $ Z_L $	56
3.7	Bode of the load impedance, $ Z_L $	56
3.8	Impedance at the PCC based on simulation tests.	57
3.9	Impedance at the PCC based on experimental tests.	57
3.10	A superimposition of the $ Z_{PCC} $ based on experimental tests using different sets of data.	58
3.11	The FDI algorithm response along with the voltage and current at the PCC.	58
3.12	NDZ of ΔP vs ΔQ for OF/UF.	62
3.13	NDZ mapping in ΔP vs ΔQ for the presented method compared with OF/UF.	62
4.1	Flow diagram depicting passive anti-islanding algorithm objective function.	68
4.2	A diagram of the architecture of the IAR with typical DG topology. .	70
4.3	The hardware of the IAR designed and constructed for online tests. .	71
4.4	The anti-island relay designed and constructed for this thesis in the sustainable power lab.	72
4.5	Single-line diagram of the simulation system.	73
4.6	A photograph of the experimental setup.	74
4.7	A photograph of the experimental setup.	75
4.8	Real time measurements of voltage and current along with contactors response in the case of island at the PCC.	76
4.9	The magnitude of $E(n,k)$ based on experimental testing.	77
4.10	The magnitude of $E(n,k)$ based on simulation.	77
4.11	The magnitude of $E(n,3)$ and $C(n)$ based on experimental tests. . . .	78

4.12	The magnitude of $F(n)$ and $C(n)$, $k=3$ based on simulation.	78
4.13	The trip signal associated with the voltage and current at the PCC.	80
5.1	A schematic diagram for the simulating system with PEC	84
5.2	A schematic diagram for the simulating system without PEC.	84
5.3	A schematic diagram for the experimental test bed system with PEC.	85
5.4	The Flowchart of Wavelet based detection.	89
5.5	Voltage and current at PCC next to the wavelet coefficients for ZIS at the condition of load matches DG output in inverter-based system.	92
5.6	Algorithm response for both normal and islanding operation and their trip signal in inverter-based system.	92
5.7	(a) Voltages at the PCC, (b) the currents at PCC, (c) the currents at EPS side, (d) the wavelet coefficients for ZIS at the condition of load, which matches the DG output in non-inverter-based system.	93
5.8	Algorithm response for both normal and islanding operation and their trip signal in non-inverter-based system.	93
5.9	Wavelet distinguish response on the condition of unbalanced load and island subjected to inverter-based system.	94
5.10	Algorithm response on the ZIS for both normal and islanding operation and their trip signal in inverter-based system.	94
5.11	Phases voltage at the PCC.	96
5.12	Phases current at the PCC.	96
5.13	The ZIS magnitude and the algorithm response and their trip signal.	96
5.14	Phases voltage at the PCC.	97
5.15	Phases current at the PCC.	97
5.16	ZIS magnitude and the algorithm response on islanding operation and their trip signal.	97

A.1	Control diagram of the inverter Model 112-60.	116
A.2	A photo of the physical inverter	117

List of Acronyms and abbreviations

AFD	Active frequency drift
DG	Distributed generation
DSP	Digital signal processing
EPS	Electrical power system
EXP	Exponential e
FFT	Fast Fourier transform
HF	High frequency
HPF	High pass filter
IM	Impedance measurement techniques
LPF	Low pass filter
NDZ	Non-Detection Zone
OF/UF	Over frequency/ Under frequency
OV/UV	Over voltage /Under voltage
PCC	Point of common coupling
PEC	Power electronic converter
PIDS	Passive islanding detection schemes
PLCC	Power line carrier communication
PWM	Pulse- width modulation

RLC	Local load
ROCFOP	Rate of change of frequency over power
ROCOF	Rate of change of frequency
ROCOP	Rate of change of output power
RPEED	Reactive power export error detection
SCADA	Supervisory control and data acquisition
SFS	Sandia frequency shift
SPD	Signal produced disconnect
SVS	Sandia voltage shift
SVS	Sandia voltage Shift
THD	Total harmonic distortion
VPS	Virtual power Signal
WPT	Wavelets packet transform
ZFT	Impedance based Fourier Transform
ZLS	Impedance based fitting
ZSI	Zero sequence impedance
ZTF	Impedance based transfer function

Chapter 1

Introduction

A new trend in modern electric power systems (EPSs) is the large-scale deployment of distributed generators (DGs) that serve as a vehicle for improving power quality, relieving transmission congestion, reducing CO₂ emissions, and increasing power availability and reliability [1]. However, large-scale deployment of DGs has significant technical challenges such as complications of responses of protection systems, power quality, stability, and islanding. The detection and removal of islanding operation are essential to ensure safe operation and to meet the interconnection standards and industrial codes. Islanding refers to a condition where a DG continues to energize a local load even though the EPS is no longer present. Adverse effects of islanding operation include low power quality, grid-protection interference, equipment damage, and safety hazards. Therefore, detecting an island has become a compulsory feature for DG integration as specified by IEEE standard and industry codes [2–4]. DG systems must be able to detect an island event and immediately de-energize the DGs, a process referred to as anti-islanding. Anti-islanding methods can be classified into two categories, remote and local. The local methods can be classified as active and passive methods [5, 6]. This thesis focuses on developing a new passive anti-islanding methodology that successfully detects the islanding event when existing

approaches fail, and complies with the interconnection standards. Passive methods are grid-friendly, simpler to implement, and inexpensive.

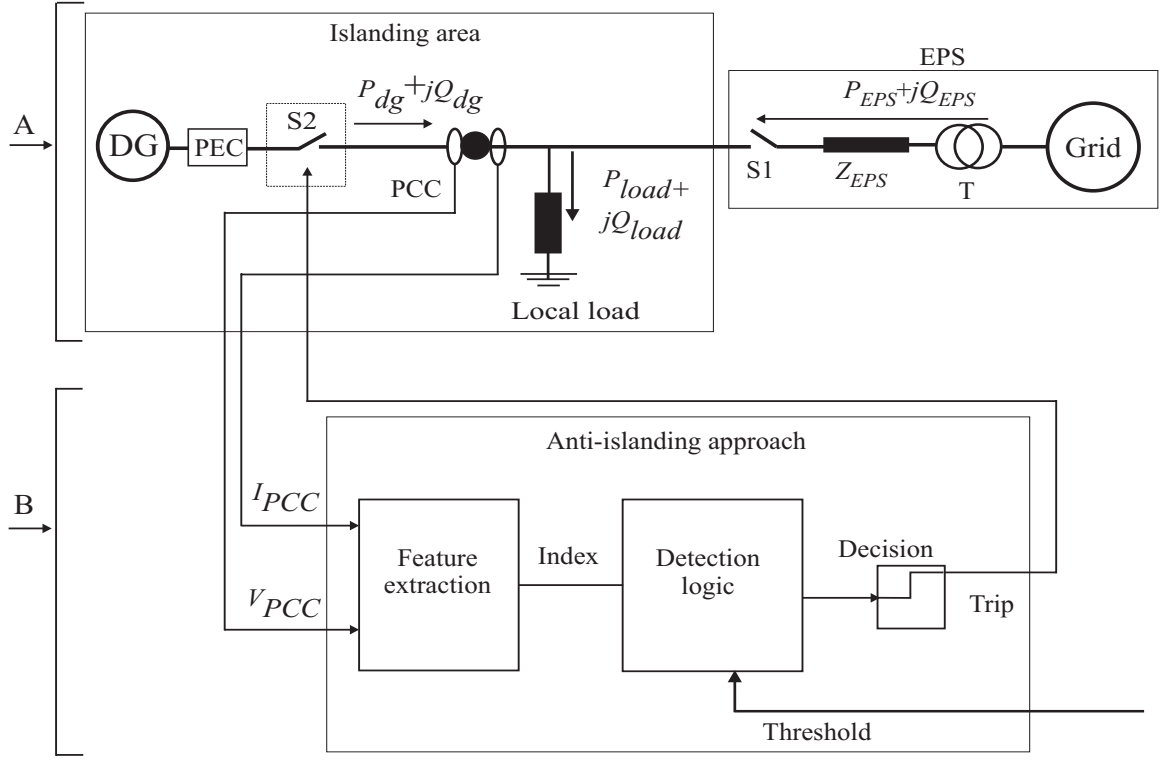


Fig. 1.1: A DG interconnection with the EPS.

A typical system topology employed to investigate the islanding phenomenon is represented in the schematic of Fig. 1.1 as defined by the 1547-IEEE standard. The system includes 1) a distributed generator (DG); 2) an electric power system (EPS); 3) a power electronic converter (PEC); 4) a point of common coupling (PCC), which is the coupling point between DG and EPS, and the point where the voltage, V_{PCC} , and current, I_{PCC} , are monitored; 5) an equivalent grid impedance (Z_{EPS}); 6) local load; 7) a circuit breaker, S1, the breaker between the EPS and DG coupled local loads, which causes islanding when opened; 8) grid connection transformer, T, and 9) circuit breaker, S2, the disconnect breaker that is triggered when islanding operation is detected. It is necessary for S2 to be open during islanding to de-energize the power-line between S1 and S2 to ensure safety of personnel who may be working on

the power-line. Furthermore, if S2 represents a distribution line breaker that opens, then S1 must be open when the automatic re-closing of S2 occurs to ensure there is no risk of damage to the DG or the EPS because the DG and EPS most likely will be out of phase at the instant of re-closing. The $P_{dg} + jQ_{dg}$ are the active and reactive power delivered by the DG, and $P_{EPS} + jQ_{EPS}$ are the active and reactive power delivered by the grid. Z_{EPS} is the equivalent grid impedance and is equal to $R + sL_g$. $P_{load} + jQ_{load}$ are the active and reactive power consumed by the local load. A general passive anti-islanding scheme as shown in Fig 1.1(B) includes 1) an index computed from features, which are based on the measurements of V_{PCC} and I_{PCC} and 2) decision logic where an index or indices are compared to the threshold. The islanding is hypothesized if the value of an index crosses a pre-specified threshold.

1.1 Problem Overview

The problem is how to use the measurements of voltage and current at the PCC, as indicated in Fig. 1.1, to determine reliably when islanding occurs. The detection is assumed to be binary¹, and it is established when a certain predefined constraints are met or violated. The requirements for the feature extraction and detection logic are being reliable and timely in removing islanding operation under all possible system operating conditions and complying with the interconnection standards. Issues that may impact the feature extraction and detection logic include measurement uncertainty² of voltage and current, harmonic distortion, power quality issues, load switching, and non-linearity effects. These result in detection errors, which may be characterized by false alarms, when no islanding occurs, but the islanding is hypothesized, and missed alarms, when islanding occurs, but is not detected. Most binary

¹Binary: islanding is present or not (0 or 1).

²Measurement uncertainty: small variations in voltage and current, and the knowledge is limited to precisely describing the sources of this influences, e.g. from the EPS that may include generator density, power system strength, operating conditions, and harmonics.

detection schemes are based on an index [7–9]. When the value of the index crosses a threshold, then islanding is hypothesised; otherwise the hypothesis is normal operation. Ideally, the index is chosen such that under all normal operating conditions, the index is restricted to some space, N , and under all operating conditions after islanding occurs, the index is restricted to some space, F , as shown in Fig. 1.2. If the spaces do not intersect, then detection is possible without false or missed alarms by choosing a threshold that lies between the two spaces. If the spaces intersect, then there is a trade-off between the number of false alarms and missed alarms depending on the choice of the threshold. Since islanding is a serious safety hazard, thresholds are usually chosen without regard to false alarm rates. In practice, when islanding

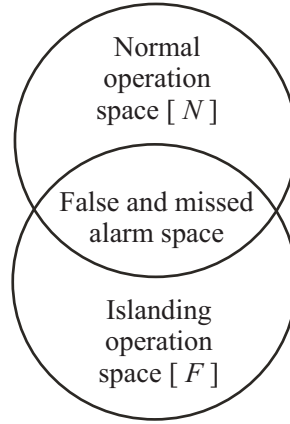


Fig. 1.2: Islanding detection challenges.

occurs, the frequency of power generation by the DG moves towards the resonant frequency of the local load. If the resonant frequency of the local load is identical or close to the grid frequency, islanding will typically not be detected by frequency based techniques [6, 10], resulting in missed alarms [11–13]. Moreover, there are two contrasting concepts about the NDZs associated with PEC based DGs and generator based DGs; the NDZs associated with PEC based DG systems are mainly influenced by the load quality factor (Q_f) and load resonance frequency. However, the NDZ shape of generator based DGs is largely influenced by detection time since these ma-

chines have a large mechanical inertia constant [14]. The performance of islanding detection schemes is not only characterized by detection error rates, but also detection latency, i.e., the time interval between the instant of islanding occurring and the instant when islanding is detected [9, 15, 16].

The challenges include how to choose an appropriate index that is insensitive to variations in V_{PCC} and I_{PCC} , which occur as a result of normal operation of the DG or EPS and local load, but is sensitive to a change in topology that results when islanding occurs. Variations in normal operation include EPS transients or DG transients, power quality events³, and measurement uncertainty. Furthermore, it is recognized that the worst case condition for islanding detection occurs when the resonant frequency of the local load is identical to the EPS frequency. It is particularly challenging to extract a feature that is sensitive to the islanding event and is not sensitive to normal operation variations. One means of establishing the effectiveness of feature extraction and detection logic relates to being sensitive to the change in topology when islanding occurs, and insensitive to normal operation thereby avoiding false alarms and missed alarms.

1.2 Literature Survey

Historically, islanding detection methods have been divided into two classes, remote and local as shown in Fig. 1.3. Each class has its own limitations and advantages [17–19]. It can be difficult to directly compare islanding detection methods, as one method may operate more effectively than another, depending on circumstances. For example, the change of terminal voltage method may be ideal for rotating machine generators due to their often large reactive component, whereas the frequency shift method works well with inverter based DGs supplying more real power. A well performing islanding identification scheme must have the ability to securely and dependably detect an

³Power quality events includes voltage sag, voltage swell, and flicker.

island event. The following is a review of the state-of-the-art of islanding detection methods for their specific advantages and disadvantages. This leads to more details of existing methods, especially the passive techniques that are related to the passive methods proposed in this dissertation.

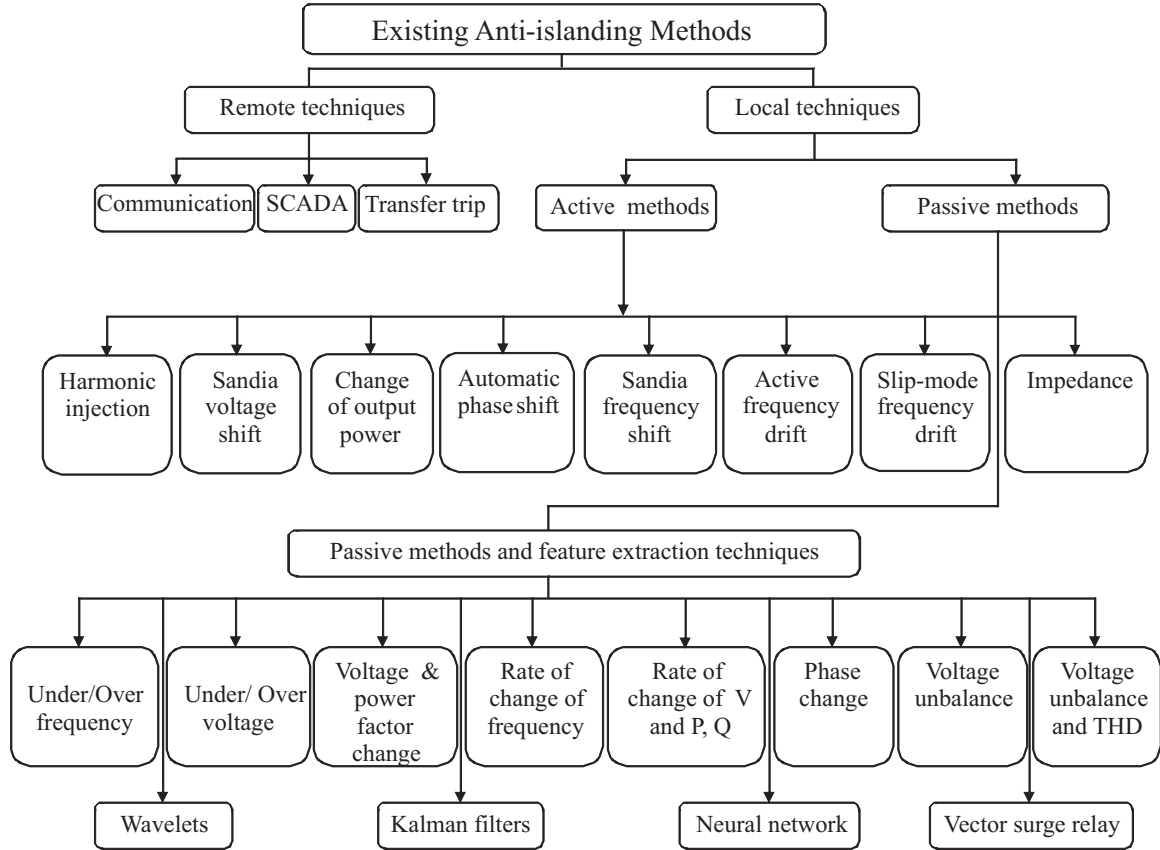


Fig. 1.3: Classification of anti-islanding methods.

Fig. 1.3 summarizes the classification of islanding detection methods found in the literature associated with data processing methods used for their feature extraction. The remote techniques include communication, SCADA, and transfer trip method. These techniques rely on communication between local DG and the EPS, which involves separate and costly communication infrastructure and protocols, especially in multi-DG systems. The remote technique does not have NDZ and does not degrade the EPS power quality. In multi-inverter systems, it is effective although

expensive to implement (especially in small systems) and has a complicated communication technique. As an example, power line carrier communication (PLCC) and signal produced by disconnect (SPD) use a low-energy communication-signal along the power-line through a transmitter that is placed near the grid protection switch and a receiver, installed at the PCC. In the absence of islanding, a low-energy signal is transmitted to the receiver and during islanding, the data transmission is stopped while ordering the PEC to trip [20]. This method is very effective in multiple-DG configurations, however, the transmitter signal must comply with several properties to ensure smooth islanding detection. This makes its application in small DG systems impractical without the involvement of the utility. Furthermore, high costs, possible/significant licensing and design complications have to be taken into account, especially for SPD, which needs a transmission of the microwave links and the telephone links [20, 21]. Moreover, a supervisory control and data acquisition system (SCADA) [22] monitors the auxiliary contacts on the utility circuit breakers to check for islanding operation. Upon islanding, a series of alarms are activated and the corresponding circuit breaker is tripped. The method is effective in detecting islanding, but it is expensive and requires many sensors that increase the complexity and the costs.

Alternatively, local techniques rely solely on the information available at the DG site, and are categorized into two types as shown in Fig. 1.3: i) active methods that rely on injecting an intentional disturbance at the PCC [6, 23–25], then using the measurements of the PCC electric signals to detect islanding, and ii) passive methods that use the measurements of electric signals at the PCC to detect presence of islanding. Although active methods have a smaller NDZ, they have a negative impact on the power quality and stability of the EPS. Most passive schemes are very cost-effective, grid-friendly, and simpler to implement, as the relays are already in place for other protection functions [26, 27]. However, the main concern is the large

NDZ that causes detection errors, especially missed alarms that become an obstacle to safe operation. The following sections give particular details on the literature most related to this research.

1.2.1 Active Anti-islanding Methods

In the active techniques, a small disturbance is injected at the PCC, and the system response is measured and used as the basis for islanding detection [28]. However, injecting a signal to the EPS adds more distortion and thus is most likely to affect the power quality, which is one of the most important considerations in power systems. Many approaches have been proposed in the literature, such as reactive power export error detection (RPEED) [29]. The essence of this approach is to force the DG system to generate a certain level of reactive power to flow to the PCC. This level of the reactive power only can be maintained when the grid remains connected. Islanding is detected when the reactive power being exported differs from a set point value for a certain interval of time. Sandia Voltage Shift (SVS) and Sandia Frequency Shift (SFS) [30], which is the accelerated version of the frequency bias method, uses positive feedback as the basis for detecting islanding operation. Automatic Phase Shift (APS) [31], is a modified SMS algorithm with additional phase shift to prevent any possible stable operating points within the UF/OF trip limits. Also, harmonic injection [32], changes of output power [33], and impedance [34, 35]. These methods give more flexibility to get more control over the NDZ that is smaller than with passive methods [12]. However, there is a possibility of deteriorating the output power quality and destabilizing the DG [36–38]. As a consequence, there is a need for further controllers for compensation, which will increase the complexity and the costs [24, 25]. An example of the active method is the impedance measurement (IM) technique that is described in the following subsection.

1.2.1.1 Impedance Technique

Two different IM's have been developed: one is the indirect approach, which measures impedance by introducing a small high frequency (HF) signal as an input to a voltage divider that is connected to the mains through a coupling capacitor [34]. The other approach is the direct method, which measures the impedance at the PCC by imposing a controlled signal to the system [35, 39]. Both approaches have their own weaknesses; in particular, the effectiveness is reduced as the number of inverters connected to the grid increases (unless all the PECs are somehow synchronized). Another necessity is to set an impedance threshold to signal that the main is connected, which requires knowledge about the value of the grid impedance that is unknown due to the complex nature of power systems. As a result, these methods have been deemed impractical [32].

1.2.2 Passive Anti-islanding Methods

Most of the passive anti-islanding methods are based on measurements of the voltage and current at the PCC that are used for feature extraction to compute an index and make a hypothesis, when the index crosses preset threshold values [40, 41]. However, the main disadvantage is the presence of a larger NDZ over which islanding detection is not possible. Over the years, a number of passive islanding detection schemes have been developed, which are based on spectral decomposition and advanced data processing filtering techniques. These techniques include the FFT, Wavelets, and Neural Networks. However, for most of these schemes, the selection of the feature, or index, and the threshold is based on heuristics⁴ and a limited set of simulations and operating conditions [7, 13, 40, 42, 43]. In addition, for most of these schemes, the characterization and assumptions are limited to a single frequency for the purpose of

⁴Heuristics: methods provide a solution that is not guaranteed to be reliable, but good enough for a given set of goals. There is no physical meaning could be provided related to the solution.

islanding detection. Nonetheless, the most common passive islanding detection methods rely on over/under voltage and frequency relays (UV/OV) and (OF/UF) possess NDZ's. These relays usually are embedded within PECs and may find applications in the DG systems that do not include PEC but with additional expense. In practice, the passive anti-islanding schemes are composed of under/over frequency relays (and their variations, e.g., rate of change of frequency (ROCOF) [44, 45], rate of change of frequency over power (ROCFOP) [5] and vector surge relays) and UV/OV relays, due to their low cost, simplicity, and availability [10, 46]. However, the reliability and accuracy of these relays, for islanding detection, need to be investigated to ensure reliable operation. The following sections provide an overview of most existing passive methods and their associated shortcomings.

1.2.2.1 UV/OV and UF/OF

The UV/OV and UF/OF relays are widely used in the power systems and their thresholds are governed by various standards [2, 3]. These relays can eliminate islanding operation using the voltage and frequency thresholds. However, IEEE 1547-2003 specifies the upper and lower voltage trip limits as 110 % and 88 %, respectively of the rated voltage, for ≤ 30 kW, and the frequency trip limits are 60.5 and 59.3 Hz [3]. With those limits, a relatively large NDZ exists for both UV/OV and UF/OF relays when they are considered for islanding detection.

In practical circumstances, there is always some power mismatch between the DG output and the load of the area EPS. This mismatch can be represented by ΔP , the active power mismatch, and ΔQ , the reactive power mismatch. During normal operation, the power mismatch will be compensated by the EPS. However, during islanding operation, the voltage and frequency will be forced to new values, V_i and f_i . When the power mismatch is large enough, V_i and f_i may be out of the nominal ranges of UV/OV and UF/OF relays and either one will trip the DG to prevent

continued islanding operation. Alternatively, if the power mismatch is not large enough to trigger one of those relays, then the operating condition is inside the NDZ and detecting islanding will fail because the mismatch of ΔP and ΔQ is too small. The UV/OV and UF/OF algorithms are governed by equations (1.1) and (1.2) [47]:

$$\left(\frac{V}{V_{\max}}\right)^2 - 1 \leq \frac{\Delta P}{P} \leq \left(\frac{V}{V_{\min}}\right)^2 \quad (1.1)$$

and,

$$Q_f \left\{ 1 - \left(\frac{f}{f_{\max}}\right)^2 \right\} \leq \frac{\Delta Q}{P} \leq Q_f \left\{ 1 - \left(\frac{f}{f_{\min}}\right)^2 \right\} \quad (1.2)$$

where $V_{\max}$, $V_{\min}$, $f_{\max}$, and $f_{\min}$ are UV/OV and UF/OF thresholds, respectively. P and Q are the active and reactive power, whereas ΔP and ΔQ are the active and reactive power mismatch at the instant of island occurrence. Q_f is the quality factor of islanding load. Typically, $V_{\max} = 110\%$ of nominal voltage, V_N , $V_{\min} = 88\%$ of V_N , $f_{\max} = 60.5$ Hz and $f_{\min} = 59.3$ Hz. Such limits result in a large NDZ, where the NDZ is more sensitive to the reactive power mismatch than it is to the active power mismatch. This method fails when the mismatched power does not reach the limits of UV/OV and UF/OF relays.

1.2.2.2 Rate of Change of Active Power

This method monitors all the changes in the power output and integrates those changes over a defined sample period. Tripping occurs when the signal exceeds the trip settings. The method can quickly detect islanding, but the disadvantage associated is basically that the active power deviation is governed by OV/UV that defines the NDZ [48].

1.2.2.3 Rate of Change of Frequency

The rate of change of frequency (ROCOF) is based on the sudden change in frequency due to the loss of mains as in [49, 50]. This method is restricted to the UF/OF as described in subsubsection 1.2.2.1.

1.2.2.4 Phase Jump Detection

This method is based on the fact that following disconnection of the grid, the phase angle between the output current and the PCC voltage is load dependent [51]. If the change in the phase angle exceeds a preset threshold, the island is detected.

1.2.2.5 Voltage and Current Harmonics

In PEC based DG systems, voltage and current harmonics have been used to detect islanding. The method proposes two parameters for islanding detection: THD and the main harmonics (3rd, 5th) of the PCC voltage, if these values exceed a specific limit, the PEC shuts down. During normal operation, the PCC voltage matches the grid voltage; hence the distortions are usually negligible because they are suppressed by the EPS; however, during islanding, two mechanisms can cause the harmonics at PCC to increase.

- Current harmonics produced by the PEC are transmitted to the load, and
- Magnetic non-linearity of the transformer causes high distortion to the voltage waveforms and increases the THD.

This method may fail in multiple DG configurations and may also fail with a high value of Q_f especially in single DG systems [27, 52].

1.2.2.6 Non-Detection Zone Characterization

In general, passive detection methods rely on the measurement of voltage and current at the PCC. They are the basis of computing an index or indices and making a hypothesis, when the index crosses preset threshold values. However, the main shortcoming is the presence of a larger NDZ over which islanding detection is not achievable. When islanding occurs, the frequency power generation at the DG moves towards the resonant frequency of the local load. The quality factor, Q_f , of the load governs the strength at which the frequency of the DG is pulled to the resonant frequency of the load. If the resonant frequency of the local load is identical or close to the grid frequency, then islanding will typically not be detected by frequency based techniques resulting in a non-zero NDZ as described by equations (1.1) and (1.2). The NDZ based on the OV/UV is mainly dominated by active power mismatch while the OF/UF is mainly dominated by reactive power mismatch [6, 28, 47, 53]. As in many cases, inductive loads are compensated with capacitors to improve the load power factor, thereby establishing a local load equivalent to a parallel of RLC circuit high quality factors and a resonant frequency that may be close to the grid frequency. Under such conditions, islanding detection, particularly passive approaches to detection, become difficult or impossible. Typically, the NDZ of islanding detection increases as Q_f increases.

Although passive anti-islanding has been explored by many researchers, some considered the islanding condition as one type of power system transient [54] and basically the schemes are employed for transient disturbance detection based on signal heuristics, while ignoring the influence of the power quality events and non-linearity. These assumptions may lead to detection errors such as missed alarms. The characterization of the change in the interconnection topology has not been sufficiently specified, and some important issues have not been addressed in the literature. Therefore, there are opportunities for innovative research. One approach addressing these issues is to

consider and capture the change in topology when islanding occurs.

This dissertation introduces an idea that could be applied practically to improve passive anti-islanding. A new methodology is presented that can detect the islanding operation at unknown operating conditions. This dissertation outlines innovative methodology, namely, frequency dependent impedance (FDI) concept that characterizes the impedance at the PCC as feature extraction. The methodology provides a new solution to islanding detection and opens a new avenue to prospective research. More details are provided in section 1.4.

In addition, the dissertation introduces a passive anti-islanding algorithm based on virtual power signal (VPS) that is proven reliable in decision making against islanding, and reducing adverse effects on the performance of grid-connected DGs. Furthermore, the time frequency dependent based index named zero sequence impedance (ZSI) is a new index introduced for islanding detection. Wavelet packet transform (WPT) is used to extract the feature. The scheme shows improved anti-islanding performance in different interconnection topologies.

1.3 Research Objective

The main research objectives are as follows:

1. To develop a new methodology that enables reliable and timely detection of islanding events under all possible operation conditions, and complies with the interconnection standards.
2. To reduce islanding detection errors by obtaining accurate, reliable islanding detection compared to existing methods, and
3. To design a hardware and software platform to implement the anti-islanding function.

1.4 Research Methodology

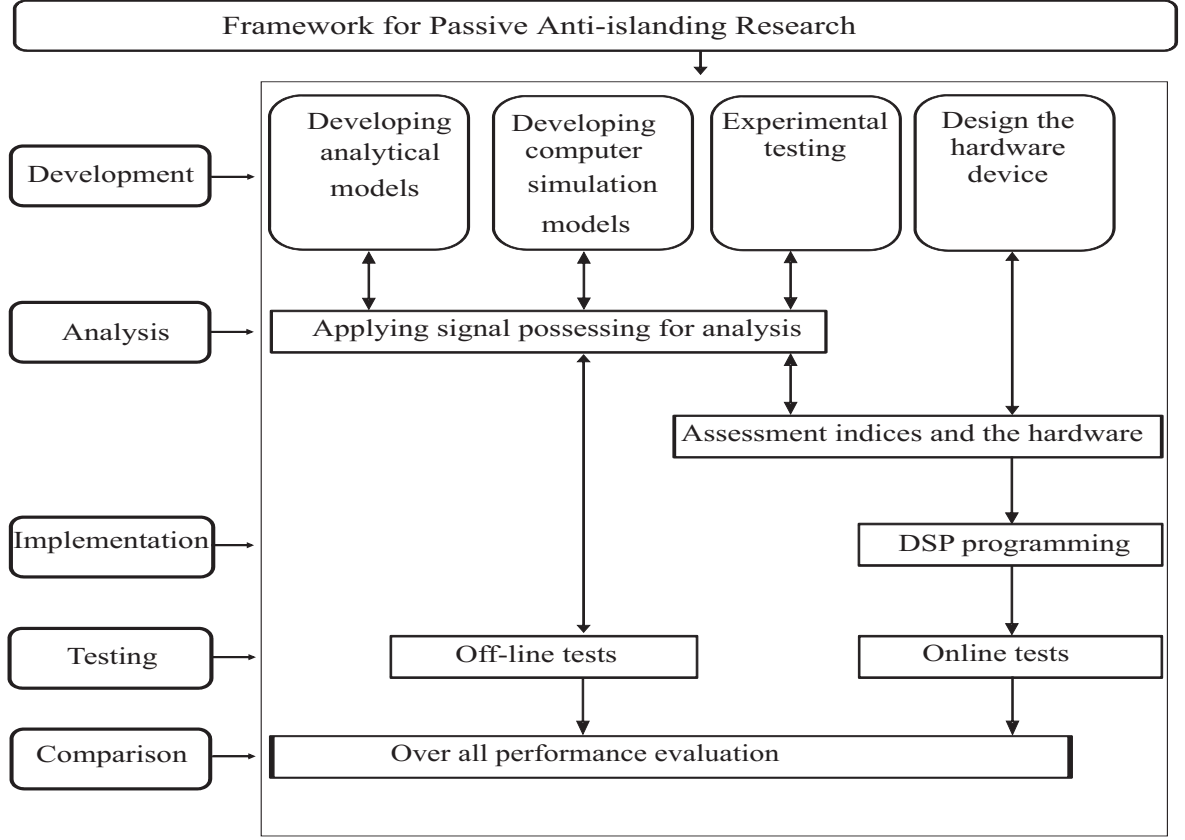


Fig. 1.4: A structure for the frame work of the proposed anti-islanding methods.

It includes developing analytical models, developing a computer simulation, building an experimental setup, and designing the hardware. The analysis stage includes data processing for feature extraction in both simulation and experiment, along with mathematical exploration. The implementation stage covers the DSP programing. The testing stage includes testing the algorithms off-line, testing the hardware and the software in a physical system, and testing the algorithm online. The comparison stage covers the evaluation of performance and comparison with existing schemes. The dissertation focuses on passive methods in order to improve islanding detection in terms of missed alarms. The measurements of voltage and current at the PCC are used to compute the FDI. The presence of the harmonic distortion in the mea-

measurements of voltage and current is used as a basis for impedance computation. The computation focuses on those frequencies where there is sufficient harmonic content, unlike the signal based techniques that rely on heuristics, which have shown a large NDZ as in [15]; consequently, missed alarms are an issue. Essentially, the methodology proposed here is based on analytical models that reflect the interconnection topology. The measured impedance characterizes the physical interconnection topology at the PCC. When islanding occurs, the interconnection changes, and this results in a change in frequency dependent impedance at the PCC. The impedance metric at various frequencies then serves as the basis for islanding detection. The impedance is chosen because it reflects the interconnect topology. Analytically, the change in interconnection topology is characterized based on a set of equations, which are derived from simple models of DG systems that include PEC and DG systems that do not include PECs. Transfer functions that characterize the physical impedance during normal and islanding operations are derived from models analytically. Features that distinguish islanding operation are extracted from the frequency response characteristics of an associated transfer function for each model. Furthermore, the frequency response characteristic is used as a basis of detection logic. The investigation includes i) establishing simple analytical models that reflect the interconnection topology, ii) characterizing the impedance variation at the PCC as a function of frequency under normal and islanding operations over a range of operating conditions, and iii) calculating metrics that depend on the frequencies of the computed impedance at the PCC, as seen from DG. Characterizing the impedance over a range of frequencies distinguishes this work over the methods that focus on the fundamental frequency such as [11]. In computer simulation, the impedance is characterized using the Fast Fourier Transforms (FFT) in spectral decomposition of the measurements of voltage and current at the PCC. The FDI concept is verified using simulation data generated using the MATLAB/SIMULINK. The essential use of simulation is to verify the feasibility

of the FDI concept and to perform a comparative analysis with existing islanding detection schemes, as well as to process the operation conditions that are unable to be processed in the lab. Furthermore, the process of fitting a transfer function model to the calculated impedance at a finite number of harmonics is presented and validated. The use of a special decomposition of measurements at the PCC is done over a range of frequencies, which provides more information at the feature extraction stage and gives the decision logic more information to make a reliable decision. This distinguishes this research from the previous schemes in which the decomposition is done in a single frequency resulting in a high missed alarm rates. The effectiveness of the FDI concept verifies experimentally that i) links the impedance derived from an interconnection topology to the impedance calculated based on the measurements of voltage and current at the PCC using simulated and experimental data, and ii) explores the validity of fitting the calculated impedance at the finite number of harmonics to the transfer function model. The main advantage of the introduced methodology is that it reduces the missed alarm rates, where the results show that it is possible to detect the islanding when the operating condition is inside the NZD of OV/UV and OF/UF schemes. This offers a chance that the methodology may be extended for use in DG systems with different interconnection topologies over different operating conditions and it may also be coupled with the active methods.

Furthermore, a new index based on the virtual power signal (VPS) is introduced, implemented using the TMS320F28335, a digital signal processor (DSP), and tested online using a new independent islanding relay that is independent from the PEC. Simulation and the experimental tests are performed for verification. The results confirm improvement in islanding detection. In addition, the hardware design is distinct due to it being specific for anti-islanding and independent from the PEC that allows it to be used in different interconnection topologies. Moreover, the ZSI as a time frequency dependent index is introduced for islanding detection. WPT [55] is used

to assess the index over various operating conditions. The validation of the index is tested in both simulation and off-line tests.

1.5 Summary of Research Contributions

This research has resulted in new passive anti-islanding methodologies that are 1) reliable, in the sense that islanding can be detected based on a frequency dependent characterization of the change of system topology, unlike signal heuristics that use the change of signal transients; 2) accurate, in the sense that the decision logic is independent of signal excitation, which reduces missed alarm rates; 3) universal, in the sense that the methodology can be extended to different interconnection topologies; and 4) independent, in the sense that the hardware is designed expressly for anti-islanding and is independent from the PEC. The research contributions of this dissertation are as follows:

- A comprehensive review of all anti-islanding techniques in the past 20 years has been completed.
- A theoretical principle is implemented and applied in practical applications that shows improvement in islanding detection as it relates to missed alarms [15]. The essence of the introduced method is based on characterizing the change in the interconnection topology rather than focusing on signal heuristics [54].
- A new passive anti-islanding methodology is presented that detects islanding events under the operating space which existing methods fail to detect [12, 14]. The frequency dependent impedance measurements distinguish this research, while [15, 35] use transient signals and focus on the fundamentals of the sinusoidal that fail to extract any useful information in some operating conditions.

- Verification of the simplified electric circuit model using simulation and experiments.
- Establishing of a passive islanding detection methodology that opens a new avenue to prospective research and it is based on an index characterized over a range of frequencies compared with [11], which focused on the simulation base of multi-indices decomposed at a single frequency.
- Reliable detection is confirmed using the measurements of voltage and current at the PCC compared with UV/OV and UF/OF [40]. In addition, the methodology aligns the analytical calculation of impedance with the results obtained from the simulation and the experimental measurements.
- The new indices, ZSI and the VPS, are introduced for passive anti-islanding that improve upon detection latency. The advantage of the ZSI index is its ability to be employed in DG systems, which include EPC and DG systems that do not include PEC compared with using the WPT as in [33], where it showed that the index is applicable to DG systems that include the EPCs only.
- Independent hardware is designed and tested online and may be used generally for islanding detection. However, most existing anti-islanding schemes are embedded within PECs as in [56]. This hardware is designed independently from the PEC, which allows it to be used in different interconnection topologies.

1.6 Dissertation Outline

The dissertation is organized as follows: Chapter 2 provides the development of analytical models, where an electric circuit model is used to derive a transfer function that characterizes the impedance during normal and islanding operations for different interconnection topologies. Chapter 3 extends the work of Chapter 2 and illustrates

FDI concept development as seen by DG, at the PCC. In addition, it shows how the impedance may be computed using the FFT of the measurements of the voltage and current at the PCC. Furthermore, it provides the fitting of the transfer function model to calculate impedance at a finite number of harmonics. Chapter 4 provides the selection, design and implementation of the VPS index, along with testing, and assessment. Chapter 5 discusses the ZSI and its assessment and limitations. Finally, summary, conclusions, and future research are highlighted in Chapter 6.

Chapter 2

A Frequency Dependent Model

2.1 Introduction

As the first step for developing a new methodology for passive islanding detection, this chapter presents a simplified analytical model that reflects the interconnection topology of DG with the EPS for i) DG systems that include EPCs and ii) DG systems that do not include EPCs. Furthermore, this chapter presents how the change of the interconnection topology can be characterized in a transfer function form. Then, frequency response characteristics of the associated transfer function are used as the basis for selecting features that distinguish the change of the interconnection topology. Finally, it is shown how the measurements of voltage and current can be used to compute the features and detect islanding operation in real time.

2.2 System Description

The DG interconnection topology shown in Fig. 1.1 consists of a local load connected at the PCC to a DG and the EPS through a breaker, S1, and grid equivalent impedance, Z_{EPS} . Islanding occurs when S1 suddenly opens. For sake of simplicity, the EPS may be represented by an ideal voltage source, V_g , in series with grid

impedance, $Z_{EPS} = R_g + sL_g$. If the EPS is a source of harmonics, such as harmonics introduced by nonlinear elements, then the harmonics are modeled as a component of V_g , which adds to the fundamental one. In the EPS, harmonics typically arise as a result of harmonics in the current caused by non-linear loads. The analysis of the EPS with non-linear loading is complex; therefore, to approximate the analysis, modeling the harmonics as a component of an ideal current source is used [32, 57, 58]. An equivalent circuit for the interconnection topology appearing in Fig. 2.1 is considered in this chapter. In this investigation, the DG is modeled as a current source, I_{dg} , as

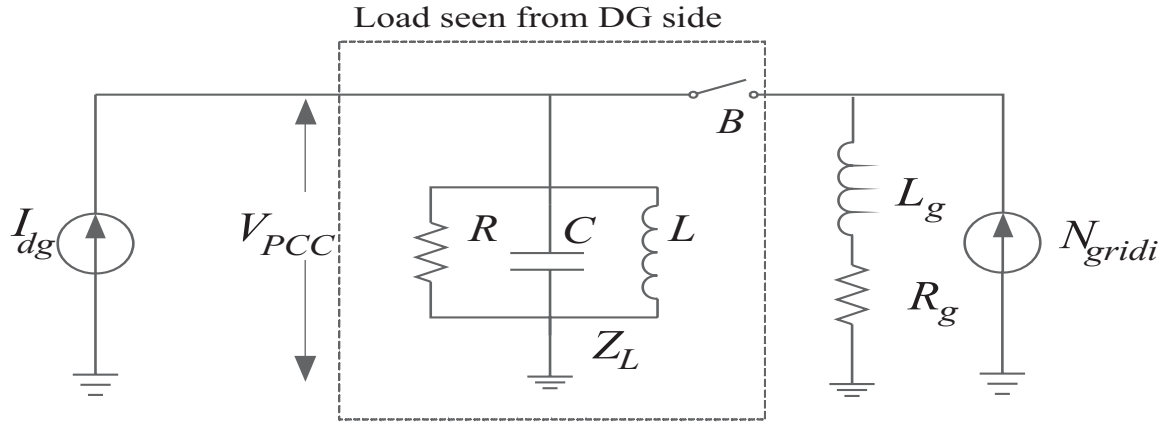


Fig. 2.1: Harmonic model of DG-EPS system without PEC.

reported [32]. The system also includes a local load, Z_L , connected at the PCC to a DG and the EPS through a breaker, B . The harmonic distortion of the EPS is represented by an ideal current source, N_{gridi} . The interconnection topology of the DG and EPS may be represented by the small signal equivalent circuit shown in Fig. 2.1 for a DG-EPS system without PEC. When the islanding operation occurs, the change in circuit topology results in a change in the impedance. The equivalent impedance, as seen by the DG, at the PCC suddenly changes from normal to islanding operation,

respectively as described by following equations:

$$Z_T(s) = Z_L(s) \left(1 + \frac{Z_L(s)}{Z_{EPS}(s)} \right)^{-1} \quad (2.1)$$

and

$$Z_T(s) = Z_L(s) \quad (2.2)$$

This results in sudden changes in the harmonic components of $i(t)$ and $v(t)$. Islanding can be detected when a sudden change is detected in measured impedance as a function of the harmonic components of V_{PCC} and I_{dg} .

A transfer function model that characterizes the relationship between voltage and current at the PCC is shown in Fig. 2.2 for a EPS-DG system based on DG systems that have a controlled EPC and DG systems that do not have EPC. As shown in Fig. 2.2, V_{PCC} denotes the harmonic distortion of the voltage at the PCC caused by the harmonics in the current sources, I_{dg} and I_{grid} .

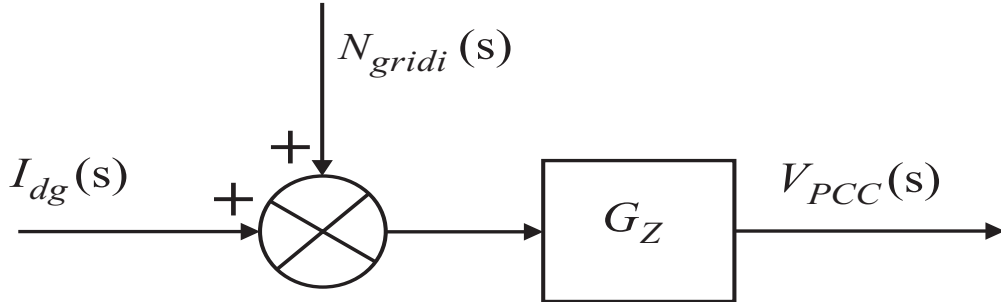


Fig. 2.2: Transfer function model of grid-DG system.

2.2.1 Hypothesis

The investigation in this chapter is conducted to characterize the frequency dependent impedance at the PCC by analytical models. These models are 1) harmonic models of grid-connected DG systems without a PEC denoted -Type-I and 2) harmonic models of grid-connected DG systems with a PEC that include i) simple harmonic

model-Type-II and ii) simple harmonic model-Type-III. The model-Type-II denotes harmonic models of a grid connected DG system with a feedback current controlled inverter and the model-Type-III denotes harmonic model of a grid connected DG system with feed forward current controlled inverter.

2.3 Simple Harmonic Model Type-I

The interconnection topology of the DG-EPS systems without a PEC, as represented by a small signal equivalent circuit shown in Fig. 2.1, is defined as model Type-I. The EPS harmonics are represented by an ideal current source. A transfer function model can be developed as illustrated in Fig. 2.2. V_{PCC} denotes the harmonic distortion of the voltage at the PCC caused by the current sources, I_{dg} and I_{grid} . When there is no islanding, V_{PCC} is represented by

$$V_{PCC}(s) = V_{PCC}^0(s) = G_Z^0(s) \left(I_{dg}(s) + N_{grid}(s) \right) \quad (2.3)$$

where the transfer function is represented by

$$G_Z^0(s) = \frac{RLL_g s(s + K)}{RLCL_g s^3 + LL_g(KRC + 1)s^2 + (KLL_g + RL_g + RL)s + KRL_g} \quad (2.4)$$

The change in impedance over a particular range of frequencies may be used as a basis for islanding detection. The impedance of Model-I, as seen by the DG, at the PCC during normal operation is defined as $Z_{PCC}^0(s) = G_Z^0(s)$. When islanding occurs, V_{PCC} is given by

$$V_{PCC}(s) = V_{PCC}^i(s) = G_Z^i(s) I_{dg}(s) \quad (2.5)$$

and

$$Z_Z^i = \frac{RLs}{RLCs^2 + Ls + R} \quad (2.6)$$

For model-I as shown in Fig. 2.1, during islanding operation, the impedance is defined as $Z_{PCC}^i(s) = G_Z^i(s)$.

The harmonic impedance can be computed from the measurements of the voltage and the current, V_{PCC} and I_{dg} , under the following conditions:

if i) there is sufficient harmonic contents in I_{dg} and V_{PCC} at complex frequencies, $s = j\omega_n, n = 1, 2, \dots$ and if ii) such harmonics are present in N_{gridi} alone; if the harmonics are present in I_{dg} alone, then the impedance at selected frequencies can be calculated at the PCC using equation (2.7):

$$|Z_{PCC}(j\omega_n)| = \frac{|V_{PCC}(j\omega_n)|}{|I_{dg}(j\omega_n)|} = |G_z(j\omega_n)|, n = 1, 2, 3, \dots \quad (2.7)$$

If the computed values of $|Z_{PCC}(j\omega_n)|$ align with $|Z_{PCC}^0(j\omega_n)|$, then the DG is operating normally. If not, then the DG is operating as an island.

2.4 PEC-Interfaced DG Systems

When a current controlled inverter is a component of the DG system, the output filters of the inverter and the nature of the feedback control within the inverter influence how the harmonics of the DG and EPS propagate to V_{PCC} and I_{dg} , and this changes the equivalent impedance, Z_{PCC} . To analyze the effect of the inverter, consider the circuit in Fig. 2.3, where the output filter of the inverter is represented by L_f , R_L , C_f , and R_c . As an example, Fig. 2.4 shows the control diagram of the current controlled EPC, including the output filter. This governs a relationship between the input, $I_{dg}(s)$, disturbances from the grid side, $N_{grid}(s)$, and the output, $V_{PCC}(s)$. This relationship can be represented by $G_Z(s)$, where the $G_Z(s)$ is the equivalent impedance of the system topology seen by the DG side at PCC. PI denotes a proportional-integral controller and Pulse-Width Modulation, PWM, switching frequency. The N_{pwmv} is denoted as the source of the harmonics inherent on the DG

side. $I_R(s)$ is the set-point of the fundamental current. There are two common ap-

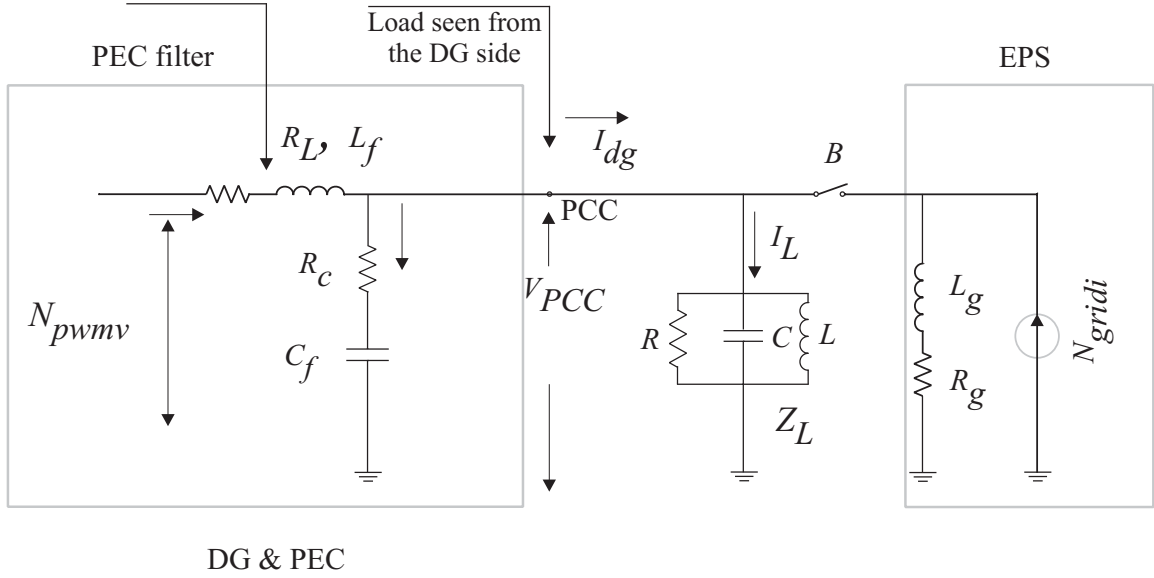


Fig. 2.3: Harmonic model of the DG-EPS system with EPC.

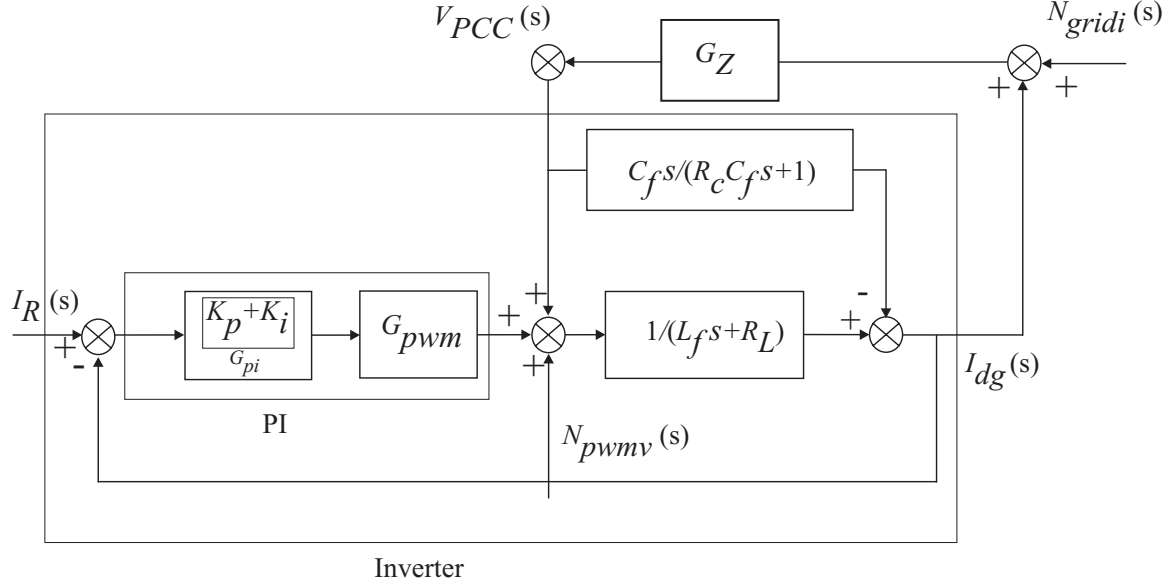


Figure 2.4: Inverter control diagram with EPS input.

proaches for the feedback control of current within the inverter: one as shown in Fig. 2.5 that represents the feedback control strategies of the inverter and the second as

shown in Fig. 2.6 that represents feed-forward control strategies of inverter. In each scenario, the controller takes the form of PI controller, $G_{PI}(s) = (sK_p + K_i)/s$, that tends to force the measured current, I_{dg} , to track the set-point fundamental current, $I_R(s)$. In Fig. 2.6, an additional term, $\frac{1}{G_{pwm}}$, that is equal to $(1/K_{pwm}) \times V_{PCC}(s)$, is

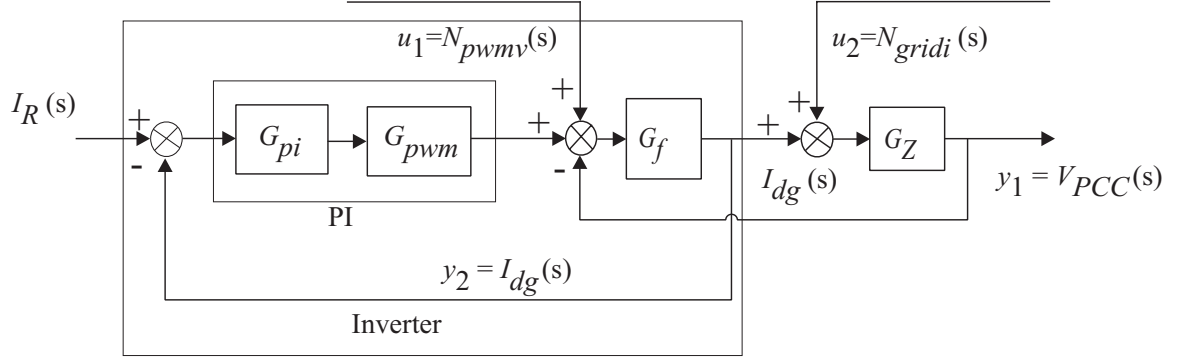


Fig. 2.5: Feedback control diagram of the inverter based DG-EPS system.

attached to the output of the PI controller to improve feedback tracking performance. The PWM switching frequency of the inverter bridge is very large compared to the fundamental frequency of 60Hz in order to reduce switching loss and improve output performance. Consequently, the PWM output over each switching interval may be modeled as a fixed value using averaging. The gain, G_{pwm} , represents the averaging effect of the PWM switching amplifier that is given by equation (2.8):

$$G_{pwm} = \frac{V_{dc}}{V_{cm}} \quad (2.8)$$

where V_{dc} is the inverter dc-bus voltage and V_{cm} is the magnitude of the carrier waveform. $G_f(s)$ represents the output filter that is given by equation 2.9:

$$G_f = \frac{1}{L_f s + R_1} - \frac{C_f s}{R_c C_f s + 1} \quad (2.9)$$

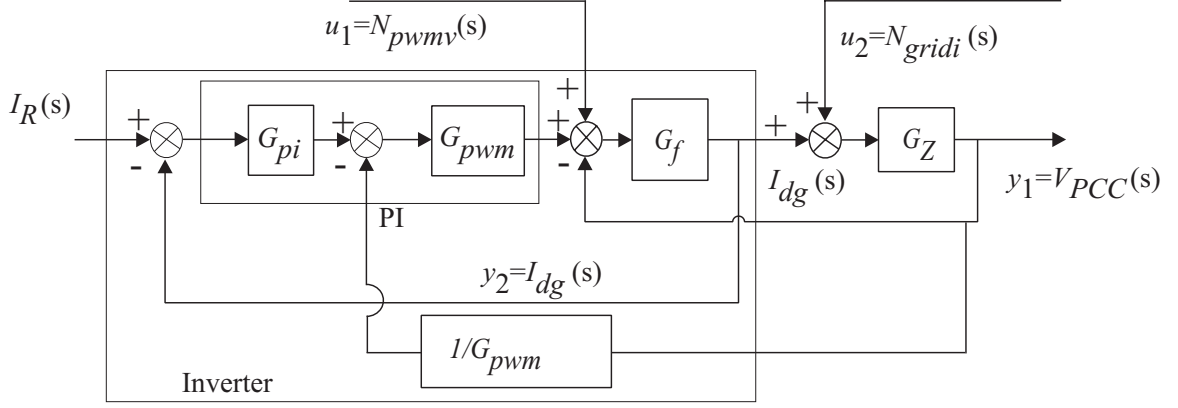


Fig. 2.6: Feed-froward control diagram of the inverter based DG-EPS system.

For Model-II and Model-III shown in Fig. 2.6 and Fig.2.5, the inputs $N_{pwmv}(s)$ and $N_{gridi}(s)$ represent the source of inherent harmonics on the DG and the EPS, while outputs include $I_{dg}(s)$ and $V_{PCC}(s)$. At the fundamental frequency, the PI controller gains and the parameters of the output filters are designed to ensure good transient and steady-state performance of the inverter. The DG acting normally can be represented by $G_Z(s) = G_Z^0(s)$, whereas the islanding operation can be represented by $G_Z(s) = G_Z^i(s)$. The following are the inverter control models that include the common approaches for the feedback current control within the inverter.

2.4.1 Simple Harmonic Model Type-II

The inverter control circuit used is represented in Fig. 2.5. Under normal operating conditions, the relationship between $V_{PCC}(s)$ and $I_{dg}(s)$ can be expressed by

$$\begin{aligned} V_{PCC}(s) &= V_{PCC}^0(s) = T_1^0(s)N_{pwmv}(s) + T_2^0(s)N_{gridi}(s), \\ I_{dg}(s) &= I_{dg}^0(s) = S_1^0(s)N_{pwmv}(s) + S_2^0(s)N_{gridi}(s) \end{aligned} \quad (2.10)$$

where,

$$\begin{aligned}
T_1^0(s) &= \frac{G_z^0(s)G_f(s)}{1 + G_{pi}(s)G_{pwm}G_f(s) + G_z^0(s)G_f(s)} \\
T_2^0(s) &= \frac{G_2^0(s) + G_{pi}(s)G_{pwm}G_f(s) + G_z^0(s)G_f(s)}{1 + G_{pi}(s)G_{pwm}G_f(s) + G_z^0(s)G_f(s)} \\
S_1^0(s) &= \frac{G_z^0(s)G_f(s)}{1 + G_{pi}(s)G_{pwm}G_f(s) + G_z^0(s)G_f(s)}
\end{aligned} \tag{2.11}$$

$$S_2^0(s) = \frac{G_z^0(s)G_f(s)}{1 + G_{pi}(s)G_{pwm}G_f(s) + G_z^0(s)G_f(s)}.$$

Depending on whether $N_{gridi} = 0$ or $N_{pwmv} = 0$, during normal operating conditions, the impedance at the PCC may be determined from V_{PCC} and I_{dg} as given by

$$\begin{aligned}
Z_{PCC}^0(s) &= \frac{V_{PCC}^0(s)}{I_{dg}^0(s)} = \frac{T_1^0(s)}{S_1^0(s)} = \left| \begin{array}{c} \\ \\ \end{array} \right|_{N_{gridi}=0}, \\
Z_{PCC}^0(s) &= \frac{V_{PCC}^0(s)}{I_{dg}^0(s)} = \frac{T_2^0(s)}{S_2^0(s)} = \left| \begin{array}{c} \\ \\ \end{array} \right|_{N_{pwmv}=0}
\end{aligned} \tag{2.12}$$

Furthermore, during islanding operation, the relationship between $V_{PCC}(s)$ and $I_{dg}(s)$ can be expressed by

$$\begin{aligned}
V_{PCC}(s) &= V_{PCC}^i(s) = T_1^i(s)N_{pwmv}(s), \\
I_{dg}(s) &= I_{dg}^i(s) = S_1^i(s)N_{pwmv}(s)
\end{aligned} \tag{2.13}$$

where,

$$\begin{aligned}
T_1^i(s) &= \frac{G_z^i(s)G_f(s)}{1 + G_{pi}(s)G_{pwm}G_f(s) + G_z^i(s)G_f(s)} \\
S_1^i(s) &= \frac{G_f(s)}{1 + G_{pi}(s)G_{pwm}G_f(s) + G_z^0(s)G_f(s)}
\end{aligned} \tag{2.14}$$

For Model-II, the impedance during islanding is given by

$$Z_{PCC}^i(s) = \frac{V_{PCC}^i(s)}{I_{dg}^i(s)} = \frac{T_1^i(s)}{S_1^i(s)} \quad (2.15)$$

2.4.2 Simple Harmonic Model Type-III

Under normal operating conditions, and based on the inverter control topology as shown in Fig. 2.6, the relationship between $V_{PCC}(s)$ and $I_{dg}(s)$ is given by

$$\begin{aligned} V_{PCC}(s) &= V_{PCC}^0(s) = T_1^0(s) N_{pwmv}(s) + T_2^0(s) N_{gridv}(s), \\ I_{dg}(s) &= I_{dg}^0(s) = S_1^0(s) N_{pwmv}(s) + S_2^0(s) N_{gridi}(s) \end{aligned} \quad (2.16)$$

where,

$$\begin{aligned} T_1^0(s) &= \frac{G_z^0(s)G_f(s)}{1 + G_{pi}(s)G_{pwm}G_f(s)} \\ T_2^0(s) &= G_z^0(s) \\ S_1^0(s) &= \frac{G_f(s)}{1 + G_{pi}(s)G_{pwm}G_f(s)} \\ S_2^0(s) &= 0. \end{aligned} \quad (2.17)$$

If $N_{gridi} = 0$, the impedance for Model-III during normal operation may be determined from V_{PCC} and I_{dg} as follows:

$$Z_{PCC}^0(s) = \frac{V_{PCC}^0(s)}{I_{dg}^0(s)} = \frac{T_1^0(s)}{S_1^0(s)} = \left| \right|_{N_{gridi}=0} \quad (2.18)$$

During islanding operation, $V_{PCC}(s)$ and $I_{dg}(s)$ are given by

$$\begin{aligned} V_{PCC}(s) &= V_{PCC}^i(s) = T_1^i(s)N_{pwmv}(s) \\ I_{dg}(s) &= I_{dg}^i(s) = S_1^i(s)N_{pwmv}(s) \end{aligned} \quad (2.19)$$

where,

$$\begin{aligned} T_1^i(s) &= \frac{G_z^i(s)G_f(s)}{1 + G_{pi}(s)G_{pwm}G_f(s)} \\ S_1^i(s) = S_1^0(s) &= \frac{G_f(s)}{1 + G_{pi}(s)G_{pwm}G_f(s)} \end{aligned} \quad (2.20)$$

For Model-III, the impedance during islanding is given by

$$Z_{PCC}^i(s) = \frac{V_{PCC}^i(s)}{I_{dg}^i(s)} = \frac{T_1^i(s)}{S_1^i(s)} \quad (2.21)$$

2.5 Assumptions for Analysis and Parameters

Standard IEEE 1547 is used as the basis for selecting the parameters of the models developed in Sections 2.3 and 2.4. The standard identifies the worst case scenario for islanding detection as follows,

- A quality factor for the local load $Q_f = R\sqrt{C/L} = 1$;
- Load resonant frequency identical to the fundamental frequency of the EPS;
and
- Zero power at the fundamental frequency supplied by the EPS, meaning the local load is fully supplied by the DG.

The local load and system parameters used for analyzing Models I, II, and III described in Sections 2.3 and 2.4 are given in Table 2.1 and Table 2.2. All the models represent a single-phase 3 kW DG system. Under normal operating conditions, the DG and EPS produce voltage and current harmonics represented by N_{pwmv} and N_{gridi} , which may influence V_{PCC} and I_{dg} , and the harmonics contained within N_{pwmv} are distinct from the harmonics contained within N_{gridi} .

Table 2.1: System Parameters

System parameter	Model I	Model II	Model III
Grid	240 V	240 V	240 V
DG	240V/3kW	240V/3kW	240V/3kW
R	16.13 Ω	16.13 Ω	16.13 Ω
L	17 mH	17 mH	17 mH
C	4110 μ F	4110 μ F	4110 μ F
L_f	2 mH	2 mH	2mH
R_L	0.2 Ω	0.2 Ω	0.2 Ω
C_f	8 μ F	8 μ F	8 μ F
K_p	10	10	10
K_i	1000	1000	1000
V_{dc}	400	400	400
V_{cm}	4	4	4

Table 2.2: Grid Impedance Parameters

$K(Rg/Lg)$	0	1	10	20	30	40
$Rg \Omega$	0	0.001	0.01	0.02	0.03	0.04
Lg mH	0.001	0.001	0.001	0.001	0.001	0.001

2.6 Analysis Results

The introduced islanding detection scheme uses changes in the frequency dependent impedance to establish whether or not islanding has occurred. The frequency response properties of the impedance is governed by the transfer functions that relate V_{PCC} to I_{dg} for Models I-III. A Bode plot of the impedance at the PCC of Model-I for normal and islanding operation is shown in Fig. 2.7, using the system parameters illustrated in Table. 2.1. The Bode of $|Z_{PCC}|$ for normal and islanding operations based on Model-I shows that: $Z_{PCC}^0(s)=G_z^0(s)$ and $Z_{PCC}^i(s)=G_z^i(s)$, as given by equations (2.3) through (2.6). When islanding occurs, depending upon the value of k ($k= Rg/Lg$), a significant increase in the impedance can be seen over the frequencies of 0.01Hz to 270Hz of around 30dB in comparison with normal operation.

Fig. 2.8 shows a Bode plot for the impedance of Model-II, where Fig. 2.8(A) represents normal operation with $N_{pwmv}=0$, Fig. 2.8(B) represents islanding operation,

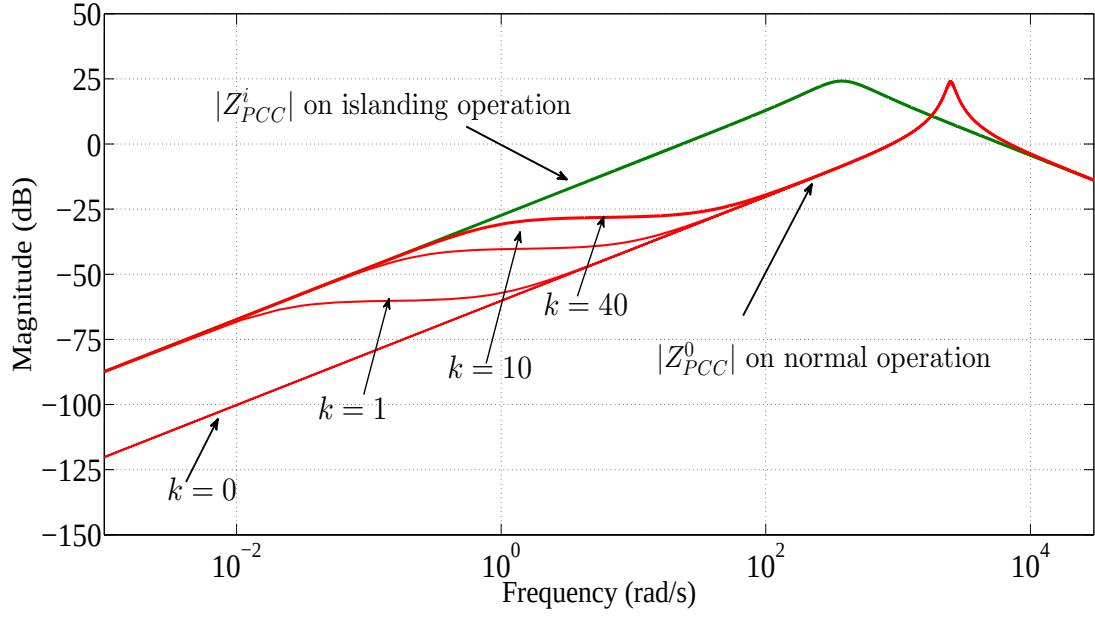


Fig. 2.7: Bode of $|Z_{PCC}|$ for Model-I in normal and islanding operation.

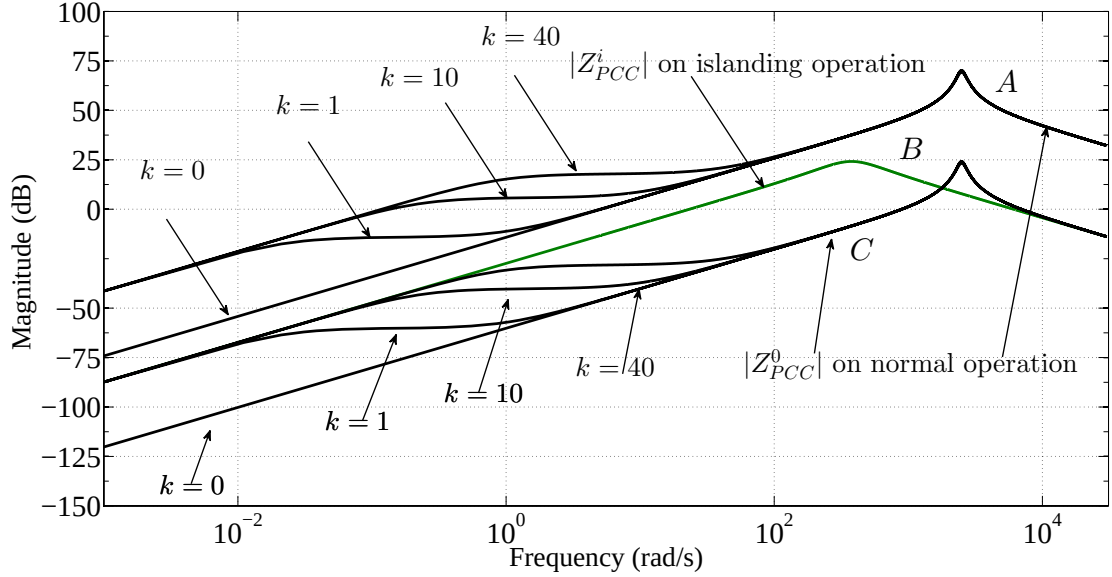


Fig. 2.8: Bode of $|Z_{PCC}|$ for Model-II in normal and islanding operation.

and Fig. 2.8(C) is the normal operation with $N_{gridi}=0$. The impedance of Model II, for normal and islanding operation is defined by

$Z_{PCC}^0(s)=T_1^0(s)/S_1^0(s)$, $Z_{PCC}^0(s)=T_2^0(s)/S_2^0(s)$, and $Z_{PCC}^i(s)=T_1^i(s)/S_1^i(s)$, as given by equations (2.12) through (2.15). When islanding occurs, depending on the value of k ($k= Rg/Lg$), a significant increase in the impedance over the frequencies of 0.01Hz to 270Hz can be seen.

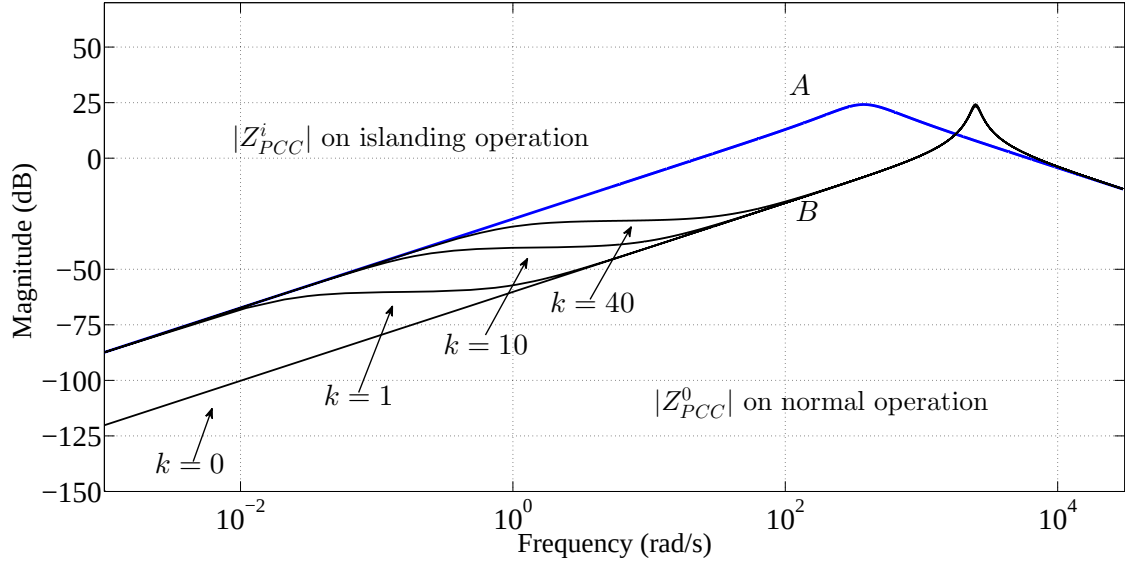


Fig. 2.9: Bode of $|Z_{PCC}|$ for Model-III in normal and islanding operation.

Fig. 2.9 shows a Bode plot for the impedance based on Model-III:

$$Z_{PCC}^0(s)=T_1^0(s)/S_1^0(s), \text{ and } Z_{PCC}^i(s) = T_1^i(s)/S_1^i(s),$$

as given by equation (2.18) and equation (2.21). When islanding occurs, depending on the value of k ($k= Rg/Lg$), a significant increase in the impedance over the frequencies of 0.01Hz to 270Hz occurs.

2.7 Impedance Based on Measurements of Voltage and Current

If one considers Fig. 2.3, it can be seen that harmonic distortions in N_{pwmv} are caused by particular harmonics in the current source, N_{pwmv} , that originate from the DG and harmonics in N_{gridi} , originating from the EPS. Such harmonics will appear in V_{PCC} and I_{dg} , as governed by the transfer functions, T_1^0 , T_2^0 , S_1^0 , S_2^0 , T_1^i , and S_1^i . In this research, a passive islanding detection based on computing the impedance, $Z_{PCC}(j\omega)$, can exploit the inherent harmonics of the measurements at the PCC of V_{PCC} and I_{dg} . When islanding occurs, the impedance suddenly changes causing an exchange in the harmonics. If the associated harmonics within N_{pwmv} are distinct from those associated with N_{gridi} and if $N_{pwmv}(j\omega) \neq 0$, then the measurements of $V_{PCC}(j\omega)$ and $I_{PCC}(j\omega)$, during islanding operation may be used to determine an impedance at a specific frequencies, $Z_{PCC}(j\omega) = V_{PCC}(j\omega)/I_{PCC}(j\omega)$. There are different scenarios that may make it characterize the source or combination of sources of particular harmonics that may impact the voltage and current measurements at the PCC. Examples of such scenarios can be stated as

- $N_{pwmv}(j\omega) \neq 0$, $N_{gridi}(j\omega) = 0$, and
- $N_{pwmv}(j\omega) \neq 0$, $N_{grid}(j\omega) \neq 0$.

In the first scenario, the measured impedance during normal operation and islanding operation represents the physical impedance that reflects the interconnection topology. In this case, the impedance computation will be based on the inherent excitation frequencies at selected harmonics. However, in the second scenario, the measured impedance does not reflect the physical impedance. Assuming that the selected frequencies, ω_n , are known, the FDI can be computed as the ratio of the FFT of V_{PCC} at ω_n to the FFT of I_{dg} at the corresponding frequencies. However, the values of

computed impedance at a particular frequency are meaningful only when there is a sufficient harmonic excitation at those frequencies. Therefore, the impedance is computed at a selected point of frequency where the magnitudes of the measured harmonics in V_{PCC} or I_{dg} are sufficiently large. Let the harmonic frequencies be denoted as

$$\omega_n = [\omega_{n_1}, \omega_{n_2}, \omega_{n_3} \dots \omega_M] \quad (2.22)$$

The impedance can be computed at each value of $\omega \in \omega_n$, as

$$|Z_{PCC}| = [|Z_{PCC}(j\omega_1)|, |Z_{PCC}(j\omega_2)|, \dots |Z_{PCC}(j\omega_M)|] \quad (2.23)$$

If selected harmonics are distinct from EPS harmonics and have non-zero values, then the index for islanding detection may be based on the magnitude of the computed impedance at multiple frequencies. If there is negligible harmonic content at a particular frequency, then it should not be included in the computation of the index. If the all harmonics are negligible, then the calculation of the index should be based only on the voltage and current measurements at the fundamental frequency only. In this case, the proposed approach is analogous to existing approaches such as [11, 13, 54] that are based on measurements of voltage, current and power at the grid fundamental frequency.

2.7.1 Approach Overview

A metric of the impedance is computed at a fixed number of frequencies where the magnitude of the harmonic in V_{PCC} and I_{dg} can be meaningfully measured and sufficiently large. Transforming the voltage and current and considering a band of frequencies, $[\omega_1, \omega_1, \dots \omega_n]$, which could be of practical consideration in using a time domain of measurements of voltage and current. Computing impedance over a band of frequencies as an index for islanding detection may be used as a basis for threshold

selection in order to detect islanding reliably. Furthermore, the band of frequencies can be selected across the resonant peak of the impedance characteristic, where islanding detection may be implemented by detecting whether or not a peak of sufficient magnitude exists in $|Z_{PCC}(\omega)|$. These scenarios are extracted based on the frequency characteristics of the associated transfer function of the introduced models, I, II, and III. A maximum impedance, $Z_{PCC}(s)$, can be seen from the Bode plots. The operation of the detection algorithm can be as shown in the flowchart in Fig. 2.10, where transit data of V_{PCC} and I_{dg} is collected every 2 sec and then the FFT for each is computed. The magnitude of the impedance is computed from the magnitude of FFT of V_{PCC} divided by the magnitude of FFT of I_{dg} at odd frequencies up to fifteen in order to define a metric of features that will be compared with a threshold. The threshold can be selected based on the Bode plot of the analytic models. Chapter 3 will illustrate more details regarding the computational approach using time domain data of simulation and real-time for evaluating the desired index.

2.8 Summary

This chapter has presented the FDI supported by analytical models that are used to derive a transfer function for the impedance. The transfer function is based on the FFT of V_{PCC} to the FFT of I_{dg} . The analytical models, I, II, and III have been illustrated and investigated to characterize the change of the interconnection topology in a transfer function form. The frequency response characteristics of the associated transfer function are then used to extract a feature to distinguish the change of the interconnection topology in case of islanding operation, and then to use the change in the impedance metric as the basis for islanding detection. Differences in impedance magnitude over a range of frequencies between normal and islanding operation are demonstrated. The impedance reflects the interconnection topology at the PCC,

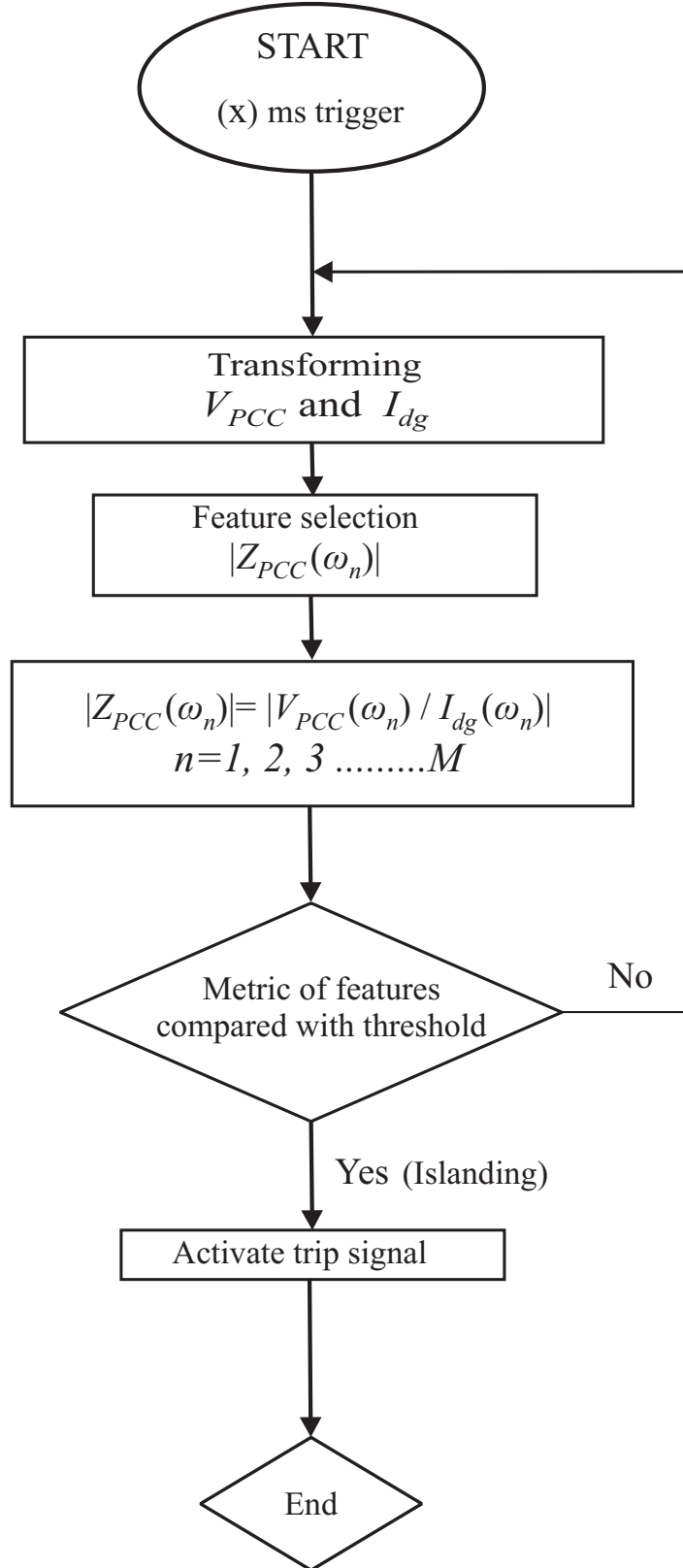


Fig. 2.10: Anti-islanding flowchart.

where the results consistently show that the shift in the resonant frequency and frequency dependent increases in the impedance can be used for islanding detection and the choice of finalizing decision thresholds. The advantage of using the FDI is its applicability for any interconnection topology. The only difference is the form of the transfer functions, T_1^0 , T_2^0 , S_1^0 , S_2^0 , T_1^i and S_1^i . Chapter 3 gives insight into the effectiveness of the presented method using simulation of realistic power system and experimental test bed. Although the use of FFT allows computing the impedance at discrete points, it may also be computed as a continuous function of frequency by fitting the discrete points to a transfer function model of impedance.

Chapter 3

Simulation and Experimental Tests

3.1 Introduction

This chapter shows that although the frequency dependent impedance may be computed at discrete points, it may also be able to be computed as a continuous function of frequency by fitting the selected points to a transfer function model of the impedance. An electric circuit model is used to analytically derive a transfer function that characterizes the impedance during normal operation and the impedance during islanding operation. Furthermore, the chapter shows how the impedance may be computed using the Fast Fourier Transform (FFT) of the measurements of the voltage and current at the PCC and how one may fit a transfer function model to the calculated impedance at a finite number of harmonics. It is then shown how the impedance pattern at various frequencies serves as the basis to detect islanding operation. In this chapter, the analytical model, simulation model, and experimental test bed are used to establish the validity of using the electric circuit model and the approach for computing the impedance at the PCC using time domain measurements of voltage and current. Finally, this chapter establishes an index for islanding detection that is based on frequency dependent impedance, along with experimental performance.

3.2 System Configurations

The analytical model, simulation model, and experimental test bed specifications are described in the following subsections.

3.2.1 Simulation Model

The MATLAB/SIMULINK SimPower Systems and Control Systems tool box were used to implement the simulation system shown in Fig. 3.1 that reflects the physical system shown in Fig. 1.1. The DG is simulated as a three-phase power supply, as provided by the SimPower Systems tool box. The parameters of the 3ϕ power supply were adjusted to the test bed power supply. The DG model was interfaced as the input to a single-phase inverter consisting of AC-DC, DC-DC, and DC-AC converters with the associated controller, as in Fig. A.1. The inverter controller was designed as detailed in [59,60]. The single phase inverter was interfaced directly to mimic the 12 kW single-phase inverter available in the lab. The simulated EPS was modeled

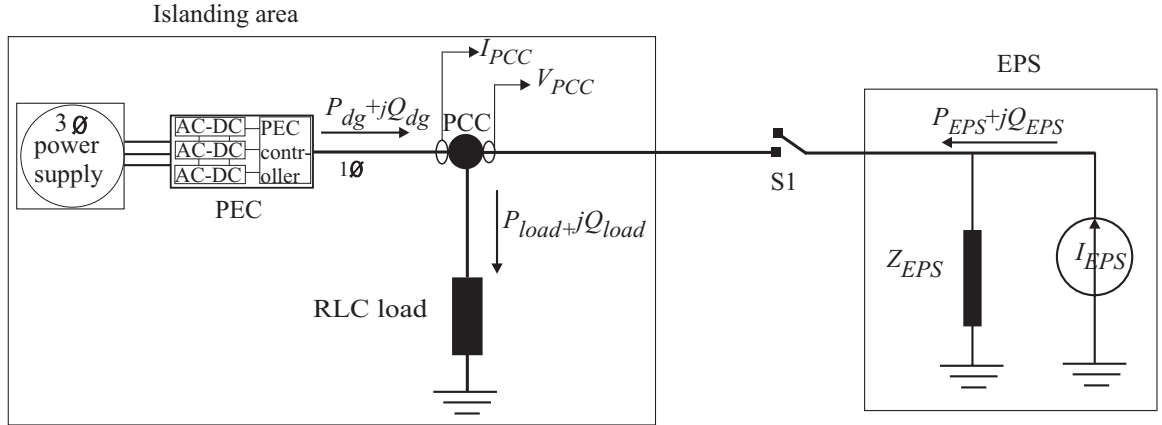


Fig. 3.1: A schematic diagram of simulation system.

by a current source in parallel with an equivalent grid impedance that is denoted by $R_g + sL_g$. The numerical values of the grid impedance used for simulation were obtained from the lab measurement data, as described in subsection 3.3.2. The local

load was modeled as a parallel resistive, capacitive, and inductive load using the SimPower Systems tool box. The single phase circuit breaker, S1, was modeled and used to create the islanding operation. The system parameters used for simulation were obtained from the test bed data and are provided in Table. 3.1.

3.2.2 Experimental Test bed

The system in Fig. 1.1 was represented by the experimental test bed shown in Fig. 3.2. The power supply of 240 V/50 A was interfaced to the input of a signal-phase inverter that was interfaced to 240/60 Hz EPS at the PCC. The local load was configured using the adjustable load Model ACLT-2430H. A circuit breaker, 240 V/50 A, was used to create islanding. Sensors for voltage and current are used as shown in the schematic diagram of the experimental test bed in Fig. 3.2. Fig. 3.3 shows a photo of the experimental setup for the 10 kW DG-EPS system used for conducting lab tests, and its parameters are listed in Table 3.1.

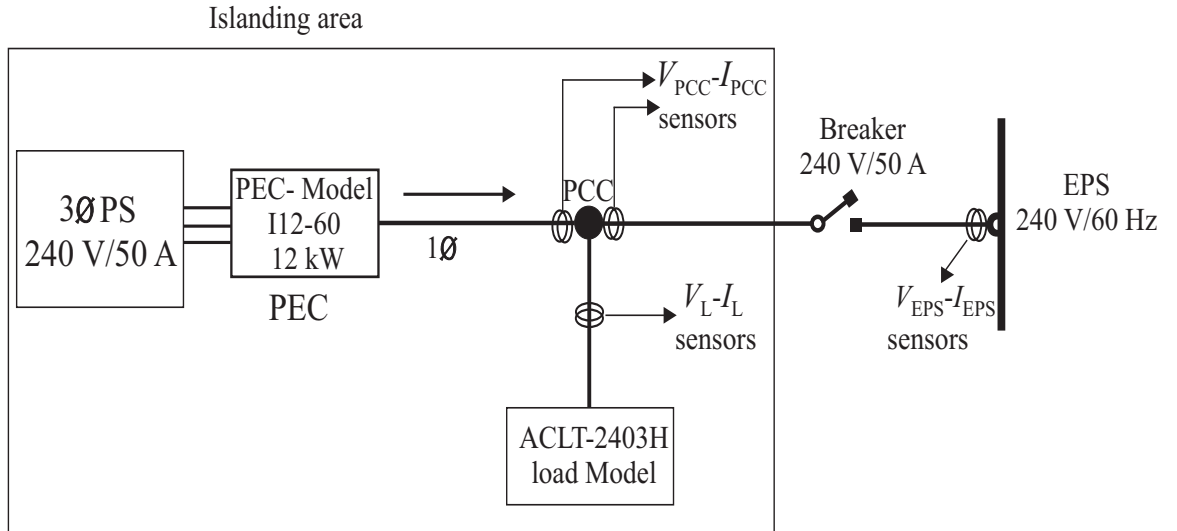


Fig. 3.2: A schematic diagram of the experimental test bed.



Fig. 3.3: A photo of the experimental setup for 10 kW DG.

3.2.3 Analytical Model

A DG-EPS interconnection topology is illustrated in the schematic diagram of the simplified electric circuit topology shown in Fig. 3.4 and consists of a linear local load, RLC, connected at the PCC to a DG and the EPS through a breaker, S1. The EPS is represented by an ideal current source in parallel with an equivalent of the grid impedance, Z_{EPS} . The voltage and current at the PCC are denoted by V_{PCC} and I_{dg} . The current through the local load is denoted by I_L . The EPS voltage and current are denoted by V_g and I_g , respectively. The equivalent impedance at the PCC, as seen by the DG both in normal and islanding operation, are denoted as Z^n and Z^i , respectively. Islanding occurs when S1 suddenly opens. This model is used to derive a transfer function, TF, that characterizes the impedance at the PCC in normal and

islanding operation as a function of frequency. The system parameters are provided in Table 3.1.

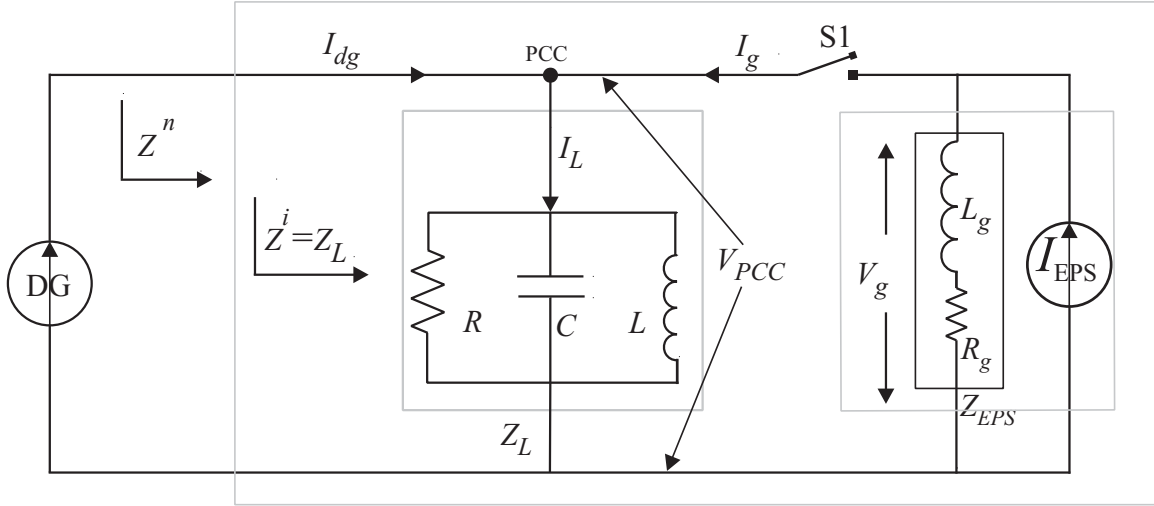


Fig. 3.4: A schematic diagram of the simplified electric circuit topology.

Table 3.1: System Parameters

Wind Emulator	10 kW
Inverter	single-phase
Type	12kW/60Hz/240V
Inverter	dual input (wind/solar) IGBT
THD	2%
RLC loads	8.27 Ω , 25.87 mH, 272 μ F
Quality factor	1
grid side	240 V, 60Hz
R_g	1.0465 Ω
L_g	0.0013 mH

3.3 Impedance-Based Analysis

In the active anti-islanding methods, an external high-frequency signal is applied on the DG side and subsequently used to measure the response signal, which is used as a basis for detecting islanding operation [12, 34, 61, 62]. However, in this research,

the impedance is characterized as a function of frequency by employing the FDI concept that uses the measurements of voltage and current at the PCC without injecting an excitation. The change in circuit topology results in a change in the impedance, where the equivalent impedance, as seen by the DG, at the PCC suddenly changes as characterized by equations (2.1) and (2.2). The impedance first is characterized as a function of frequency using an electrical circuit model shown in Fig. 3.4; then the experimental tests are conducted for both normal and islanding operation in order to estimate the grid impedance. The obtained numerical values of the grid impedance can be used in the simulation of the realistic power system shown in Fig. 3.1. The impedance at the PCC is characterized using the FFT techniques. The grid impedance is estimated from the impedance during normal and islanding operation. The numerical values of the local load are obtained from tests conducted in the lab, then are further used in the electrical circuit model. The simulation model is used for validation, where it may provide more flexibility for measurements that are not accessible in a physical system. The impedance at selected frequency, $Z(j\omega)$, can be calculated from $V(j\omega)/I(j\omega)$, if measurements of $V(j\omega)$ and $I(j\omega)$ are available. The following subsections give details representing the mathematical exploration and describe the steps for validation by considering three methods to compute the equivalent impedance that provide the support and validate the introduced methodology. The three different equivalent impedance calculation include i) impedance based network topology, ii) impedance based on FFT, and iii) fitting impedance measurements to transfer function model. A notation has been developed to distinguish the context of the impedance as it related to the equivalent impedance in electrical circuit model or calculation of an impedance using time series measurements of voltage and current. In the context of equivalent electrical circuit impedance, the notation is $Z^{nA}(s)$ and $Z^{iA}(s)$, where i denotes islanding topology, n denotes normal topology, and A denotes the context. In the context of the impedance based on FFT of time series measure-

ments; the notation is $Z^{nB}(j\omega_m)$ and $Z^{iB}(j\omega_m)$, where B is the context and m is the FFT discrete point, $m = 1, 2, \dots, N$. In the context of the impedance based on fitting impedance measurement to a transfer function model, the notation is $Z^{nC}(s)$ and $Z^{iC}(s)$, where C is the context.

Assuming the measurements of $I_{dg}(j\omega)$ and $V_{PCC}(j\omega)$ are available at the calculated set of frequencies, $\omega \in [\omega_1, \omega_2, \dots, \omega_n]$, the $V_{PCC}(j\omega)$ and $I_{PCC}(j\omega)$ are estimated from the FFT of the time domain record of $V_{PCC}(t)$ and $I_{dg}(t)$.

If $I_{dg}(j\omega_n) \neq 0$ and $I_g(j\omega_n) = 0$, then the impedance derived during normal and islanding operation can be represented by

$$\frac{V_{PCC}(j\omega)}{I_{dg}(j\omega)} = \frac{Z_L(j\omega)Z_{EPS}(j\omega)}{Z_{EPS}(j\omega) + Z_L(j\omega)} \quad (3.1)$$

and

$$\frac{V_{PCC}(j\omega)}{I_{dg}(j\omega)} = Z_L(j\omega) \quad (3.2)$$

This suggests that the difference in $Z_L(j\omega)$ and, $Z_L(j\omega)Z_{EPS}(j\omega)/Z_{EPS}(j\omega) + Z_L(j\omega)$ can be represented by the difference, ΔZ , and it may be used as a basis for islanding detection, where the ΔZ can be defined by

$$\Delta Z = Z_L - \frac{Z_L Z_{EPS}}{Z_L + Z_{EPS}} = \frac{Z_L(j\omega)}{1 + \frac{Z_{EPS}(j\omega)}{Z_L(j\omega)}} \quad (3.3)$$

3.3.1 Impedance Based Network Topology (ZTF)

The transfer function derived in equations (2.4) and (2.6) may characterize the impedance during normal and islanding operation. The impedance magnitude, as seen from the DG side, can be calculated from the transfer function as given in equation (3.4), where it represents the impedance during the islanding operation. The frequency response of associated transfer function can be compared to that computed from the time series data determined from simulation and test-bed experiments. The

voltage, current, and power in the RLC load were measured during the experimental tests when the circuit breaker, S1, was opened. The measured voltage and current are used as the basis to compute the numerical values of load and both appear in Table 3.1.

$$Z^{iA}(s) = H(s) = \frac{RLs}{RLCs^2 + Ls + R} \quad (3.4)$$

3.3.2 Grid Impedance Estimation

The purpose of estimating Z_{EPS} from the experimental tests is to substitute it into the simulation model, in order i) to generate a model for grid impedance that mimics the actual physical grid impedance in the lab and ii) to investigate the impact of the change on the Z_{EPS} over a range of frequencies and how this change impacts the proposed methodology. From the electrical circuit model shown in Fig. 3.4, during normal operation, $Z^n = Z_{EPS} // Z_L$. However, during islanding operation, $Z^i = Z_L$. The mathematical derivation of the impedance can be seen in equations (3.5) to (3.9), which are used to estimate an equivalent of grid impedance. $Z_L(s)$ denotes the local load impedance as a function of frequency, and it is equal to the islanding impedance as well. Z_{EPS} can be computed as, the impedance from the DG, based on equations (3.5) to (3.9), as

$$Z^n(s) = Z_{PCC}(s) = \frac{Z_{EPS}(s)Z_L(s)}{Z_{EPS}(s) + Z_L(s)} = \frac{Z_L(s)}{Z_L(s)/Z_{EPS}(s) + 1} \quad (3.5)$$

$$Z_{EPS}(s) = \frac{Z_L(s)Z_{PCC}(s)}{Z_L(s) - Z_{PCC}(s)} \quad (3.6)$$

The impedance can be defined as a complex value, $\Re + j \Im$, and by replacing (s) with $(j\omega)$, it can be rewritten as Z_{PCC} and Z_L by substituting as follows:

$$\begin{aligned} Z_{PCC}(j\omega) &= a(j\omega) + b(j\omega) \\ Z_L(j\omega) &= c(j\omega) + jd(j\omega) \end{aligned} \quad (3.7)$$

$$Z_{EPS} = \frac{(ac - db) + j(da + bc)}{(c - a) + j(d - b)} = \frac{N_{\Re} + jN_{\Im}}{D_{\Re} + jD_{\Im}} \quad (3.8)$$

Z_{EPS} can be deduced and can be rewritten as

$$Z_{EPS} = \frac{N_{\Re}D_{\Re} + N_{\Im}D_{\Im}}{(D_{\Re})^2 + (D_{\Im})^2} + j\frac{N_{\Im}D_{\Re} - N_{\Re}D_{\Im}}{(D_{\Re})^2 + (D_{\Im})^2} \quad (3.9)$$

3.3.3 Impedance Based on FFT Technique (ZFT)

The measurements of voltage and current at the PCC may contain the fundamental harmonic and the background harmonics that may be derived from either DGs or the EPS. In general, the mathematical time representation that describes a periodic signal, $x(t)$ can be expressed by equation (3.10):

$$x(t) = \sum_{k=1}^{\infty} |X(k\omega_0)| \cos(k\omega_0 t + \varphi(X(k\omega_0))) \quad (3.10)$$

The signal $x(t)$ could be a measured signal of V_{PCC} , V_L , V_g , I_{dg} , I_L , or I_g . The term $X(k\omega_0)$ is the frequency representation of the signal $x(t)$, and it is computed using the discrete Fourier transform as in equation (3.11):

$$\begin{aligned} X(k\omega_0) &= \sum_{n=0}^{N-1} x(hT) e^{-jk\omega_0 nT} \\ &= \Re(X(k\omega_0)) + j\Im(X(k\omega_0)) \end{aligned} \quad (3.11)$$

where T , N , and ω_0 are the sampling time, the length of the discrete signal $x(hT)$, and the fundamental frequency in rad/s , respectively. Here, $k \in [1, 2, \dots, \infty]$ represents the harmonic order; however, in practice k is limited to an integer number, M . The terms $|X(k\omega_0)|$ and $\varphi(X(k\omega_0))$ are the magnitude and the phase of the signal $X(k\omega_0)$, whereas $\Re(X(k\omega_0))$ and $\Im(X(k\omega_0))$ are the real and the imaginary value of the signal $X(k\omega_0)$. An impedance, Z , can be expressed as a ratio of the voltage and the current,

as in equation (3.12):

$$Z = \frac{V}{I} \quad (3.12)$$

Furthermore, the computed impedance at multiple frequencies, $Z(k\omega_0)$, is given by

$$Z(k\omega_0) = \frac{V(k\omega_0)}{I(k\omega_0)} = \Re(Z(k\omega_0)) + j\Im(Z(k\omega_0)) \quad (3.13)$$

where $V(k\omega_0)$ and $I(k\omega_0)$ are the frequency representation of the voltage and current signals, computed using equation (3.11). Following equation (3.13), the impedance magnitude, $|Z(k\omega_0)|$, at different frequencies is given by

$$|Z(k\omega_0)| = \frac{|V(k\omega_0)|}{|I(k\omega_0)|} = \sqrt{(\Re(Z(k\omega_0)))^2 + (\Im(Z(k\omega_0)))^2} \quad (3.14)$$

3.3.4 Fitting Impedance Measurements to Transfer Function Model (ZLS)

Although impedance is computed at discrete points, it may also be computed as a continuous function of frequency by fitting the discrete points to a transfer function model of the impedance. This can be done by estimating the transfer function of the impedance in terms of numerator and denominator. The transfer function coefficients are computed by equations (3.15) to (3.18). A least squares method is used. This is a statistical method used to determine the line of best fit by minimizing the sum of squares created by a mathematical function as follows:

The transfer function of the impedance can be estimated based on the measured voltage and current at any point of the system based on equation (3.15):

$$Z(s) = \frac{V(s)}{I(s)} = \frac{n(s)}{d(s)} \quad (3.15)$$

where $s = j\omega = jk\omega_0$, and the impedance Z could be load impedance, Z_L , the impedance at the PCC or grid impedance, Z_g . For example, the load impedance and impedance at the PCC can be found by estimating the transfer function coefficients, as in equation (3.16):

$$Z_L(s) = \frac{n_L(s)}{d_L(s)}, \quad Z_{PCC}(s) = \frac{n_{PCC}(s)}{d_{PCC}(s)} \quad (3.16)$$

where

$$\begin{aligned} n(s) &= a_0 + a_1s + a_2s^2 + \dots + a_Ms^M, \\ d(s) &= 1 + b_1s + b_2s^2 + \dots + b_Ms^M \end{aligned} \quad (3.17)$$

The $n(s)$ and $d(s)$ are the numerator and denominator polynomials characterized by coefficients. Equation (3.9) can be rearranged based on the real and imaginary values, as in equation (3.18):

$$\Re(n(s)) + j\Im(n(s)) = \Re(d(s)Z(s)) + j\Im(d(s)Z(s)) \quad (3.18)$$

The calculation can be obtained by minimizing the least squares error:

$$\begin{aligned} \Re[Z(jk\omega_0)d(jk\omega_0) - n(jk\omega_0)] &= \varepsilon_k, \quad k = 1, 2, \dots, M \\ \Im[Z(jk\omega_0)d(jk\omega_0) - n(jk\omega_0)] &= \varepsilon_{k+M}, \quad k = 1, 2, \dots, M \end{aligned} \quad (3.19)$$

where, if j is omitted, the above equation can be rewritten as equation (3.20):

$$\begin{aligned} \Re[Z(k\omega_0)d(k\omega_0) - n(k\omega_0)] &= \varepsilon_k, \quad k = 1, 2, \dots, M \\ \Im[Z(k\omega_0)d(k\omega_0) - n(k\omega_0)] &= \varepsilon_{k+M}, \quad k = 1, 2, \dots, M \end{aligned} \quad (3.20)$$

where $Z(k\omega_0)$ is defined in (3.13). Equation (3.20) can be simplified as in equation (3.21):

$$\Psi p - \Gamma = \varepsilon, \quad (3.21)$$

where

$$p = [a_0 \ a_1 \ \dots \ a_M \ b_1 \ b_2 \ \dots \ b_M]^T, \quad (3.22)$$

$$\varepsilon = [\varepsilon_0 \ \varepsilon_1 \ \dots \ \varepsilon_{2M}]^T,$$

$$\Psi = \begin{bmatrix} A(\omega_0) \\ \vdots \\ A(\omega_n) \end{bmatrix} p, \text{ and } \Gamma = \begin{bmatrix} B(\omega_0) \\ \vdots \\ B(\omega_n) \end{bmatrix} \quad (3.23)$$

where $A(\omega_i) \in \mathbb{R}^{2 \times (2n+1)}$ and $B(\omega_i) \in \mathbb{R}^{2 \times 1}$ results from equal the left, the real, and the imaginary of equation (3.19) and ω_i denotes the frequency. The variables p represent the polynomial of the transfer function $H(s)$ to be estimated. The least squares solutions that minimize ε^T are given by

$$p = (\Psi^T \Psi)^{-1} \Psi^T \Gamma,$$

provided that

$$\det(\Psi^T \Psi) \neq 0 \quad (3.24)$$

For a second order system, the matrices A, B, and X are given by

$$A(\omega_i) = \begin{bmatrix} 1 & 0 & -\omega_i^2 & -\Re(Z(\omega_i)) & \Im(Z(\omega_i)) \times \omega_i \\ 0 & \omega_i & 0 & -\Im(Z(\omega_i)) & -\Re(Z(\omega_i)) \times \omega_i \end{bmatrix} \quad (3.25)$$

$$B(\omega_i) = \begin{bmatrix} -\Re(Z(\omega_i)) \times \omega_i^2 \\ \Im(Z(\omega_i)) \times \omega_i^2 \end{bmatrix} \quad (3.26)$$

$$p = \begin{bmatrix} a_0 & a_1 & a_2 & b_0 & b_1 \end{bmatrix}^T \quad (3.27)$$

3.4 Implementing the ZFT Based Anti-islanding Method

The difference in the equivalent impedance during normal and islanding operation as demonstrated by equation (3.3) is used as a basis of islanding detection. The magnitude of impedance at the PCC for the selected frequency points, computed using equation (3.14) during normal and islanding operation, is rewritten as a metric of impedance;

$$z_k = |Z(k\omega_0)| \quad (3.28)$$

where $k \in [1, \dots, M]$ and denotes the harmonic order.

A metric of impedance at selected frequencies where a sufficient harmonic content exists, is defined by

$$Z_T = \sqrt{\sum_{r \subset k}^M z_r^2} \quad (3.29)$$

where $r \subset k$, and $k \in [1, \dots, M]$ and r introduces only odd harmonics up to 15. The metric of the impedance during normal operation is defined by Z_T^n , and the metric of the impedance during islanding operation is defined by Z_T^i . The index is chosen as Z_T . The threshold, β , is selected at the midpoint between the Z_T^n and Z_T^i . The value of β is mathematically obtained by

$$\beta = \frac{1}{2}(Z_T^n + Z_T^i) \quad (3.30)$$

Fig. 4.4 shows the algorithm flowchart that describes the process of the proposed approach for the anti-islanding detection. The process is based on computing the impedance based on the measurements of voltage and current at the PCC. The is-

landing can be detected by computing the complex impedance at selected frequencies as in the following steps:

STEP 1: initialize the samples index $m=0$;

STEP 2: read each sample of voltage and current at the PCC of window $m=\alpha$, where α is the number of samples and represents the size of the buffer;

STEP 3: synchronize the computation of the real and imaginary values of voltage and current based on the FFT as denoted in equations (3.12) and (3.14) with the same α ;

STEP 4: determine the magnitude of the impedance as a complex value for selected harmonics at each given sample as given in equation (3.14); and

STEP 5: if the magnitude of z_r that is given by equation (3.29) at any of the chosen frequencies lies beyond the Z_T as described by equation (3.29), then islanding must be automatically declared by activating the trip signal. Otherwise, $m=m+1$ by adding one sample of voltage and current, and the process returns to step 2.

$$\text{For } Z_T = \begin{cases} 1 \rightarrow & \text{Islanding operation} \\ 0 \rightarrow & \text{Normal operation} \end{cases}$$

The trip signal will activate the control circuit, which will disconnect the DG as the islanding is detected.

3.5 Results and Discussion

Both simulation and experimental tests were conducted using the power system shown in Fig. 1.1 and described in section 3.2. The tests were conducted to investigate the worst case islanding scenarios, where line-voltage and frequency were held within the normal levels even after the islanding event. In addition, the active and reactive power were kept at zero from the EPS. This extreme situation was considered within

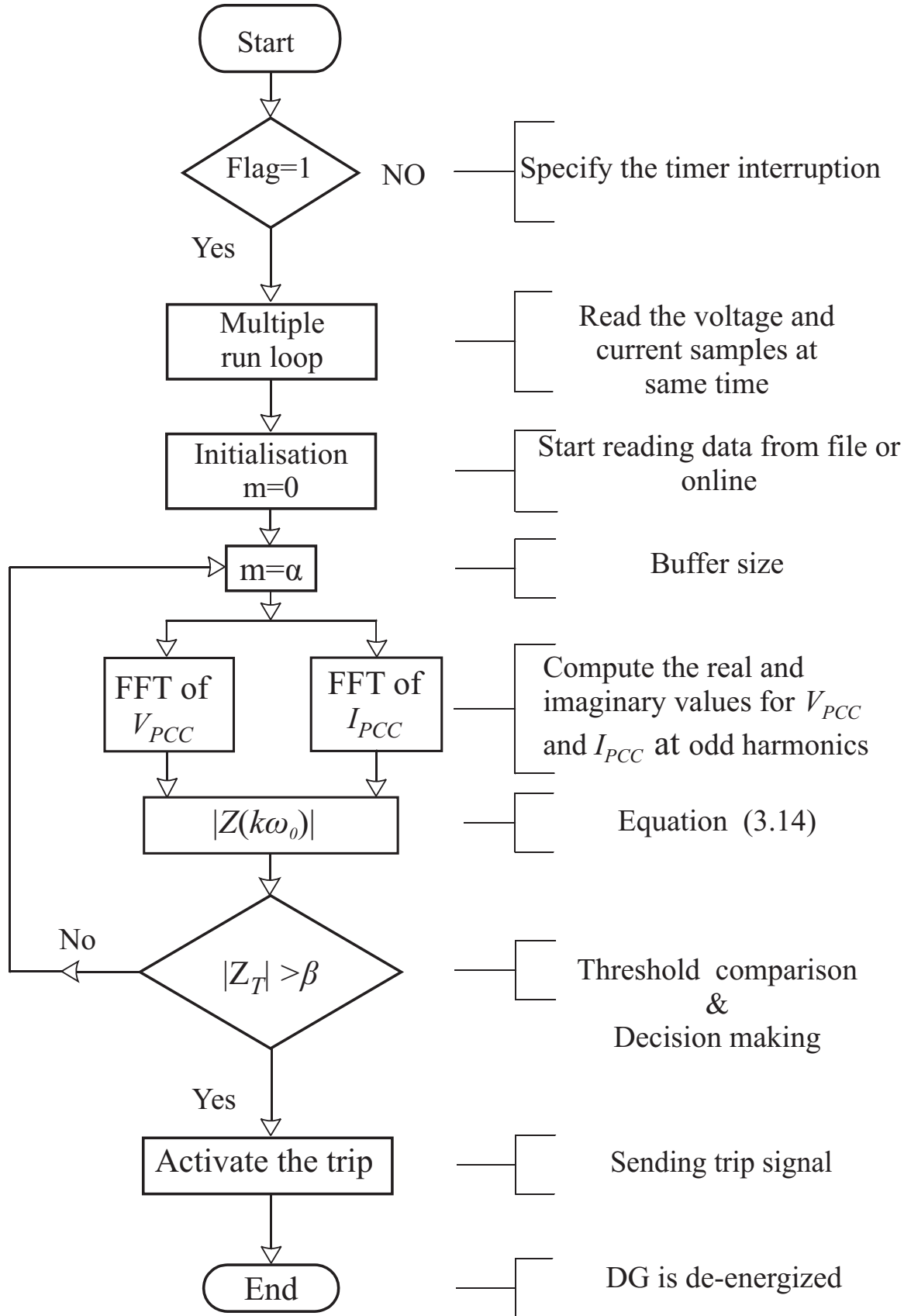


Fig. 3.5: Flow diagram depicting the passive anti-islanding algorithm for the objective function.

the simulation as well as in the experimental tests. Furthermore, the system was modeled by an equivalent signal-line diagram, as shown in Fig. 4.2. In this work, the simulation and the experimental tests were conducted under the following conditions:

- the resonant frequency was the same as the grid frequency;
- the load quality factor was kept at 1; and
- the load active and reactive power consumed from the grid were kept close to zero, where the ΔP and ΔQ power mismatches were maintained at zero.

Fig. 3.6 represents a superimposed magnitude of load impedance, Z_L , based on parametric calculation and the measurement data of normal and islanding operation over a range of frequencies. Fig 3.7 represents the Bode of Z_L based on fitting the measurements data to a transfer function model in normal and islanding operation, along with the Z_L based on parametric calculations. Fig. 3.6 and Fig 3.7 show the validity of the introduced algorithm.

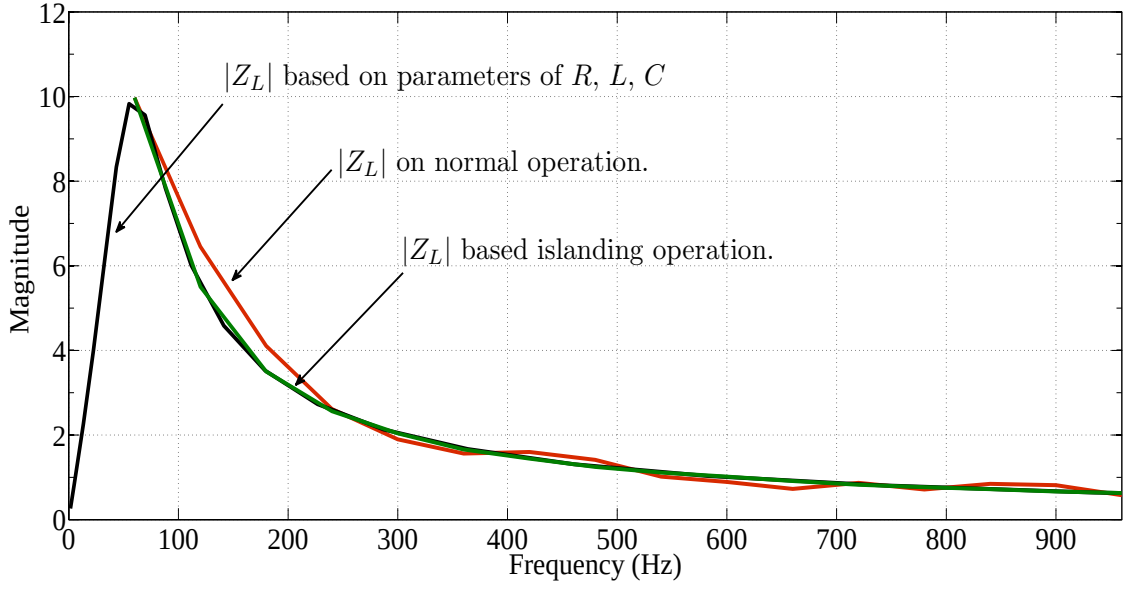


Fig. 3.6: Superimposed of the load impedance, $|Z_L|$.

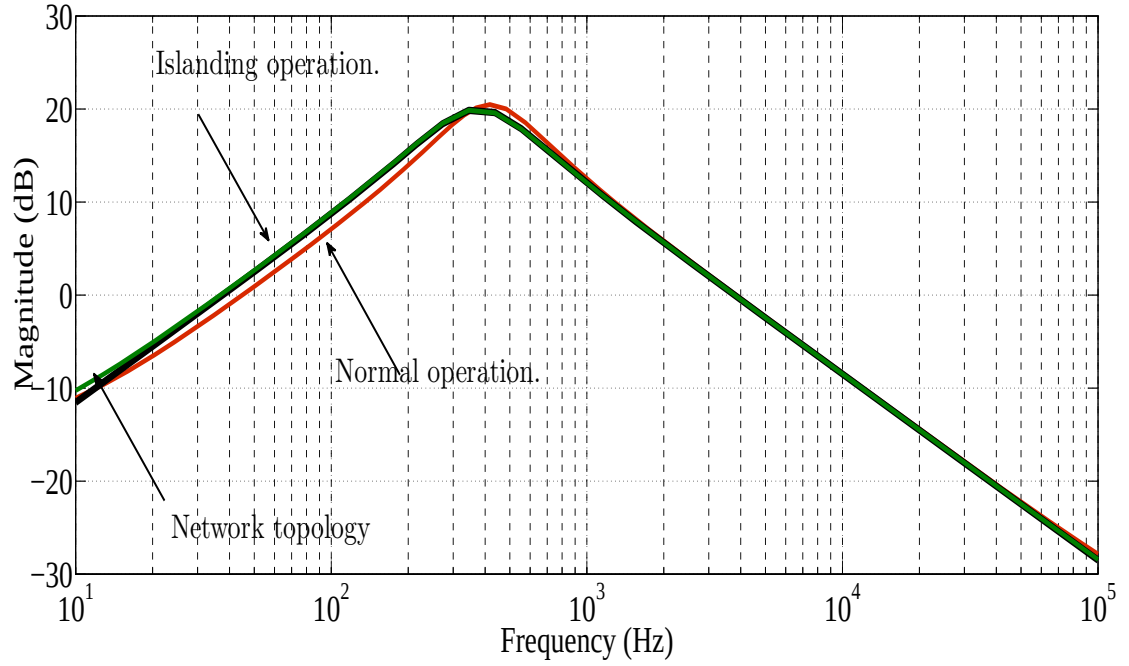


Fig. 3.7: Bode of the load impedance, $|Z_L|$.

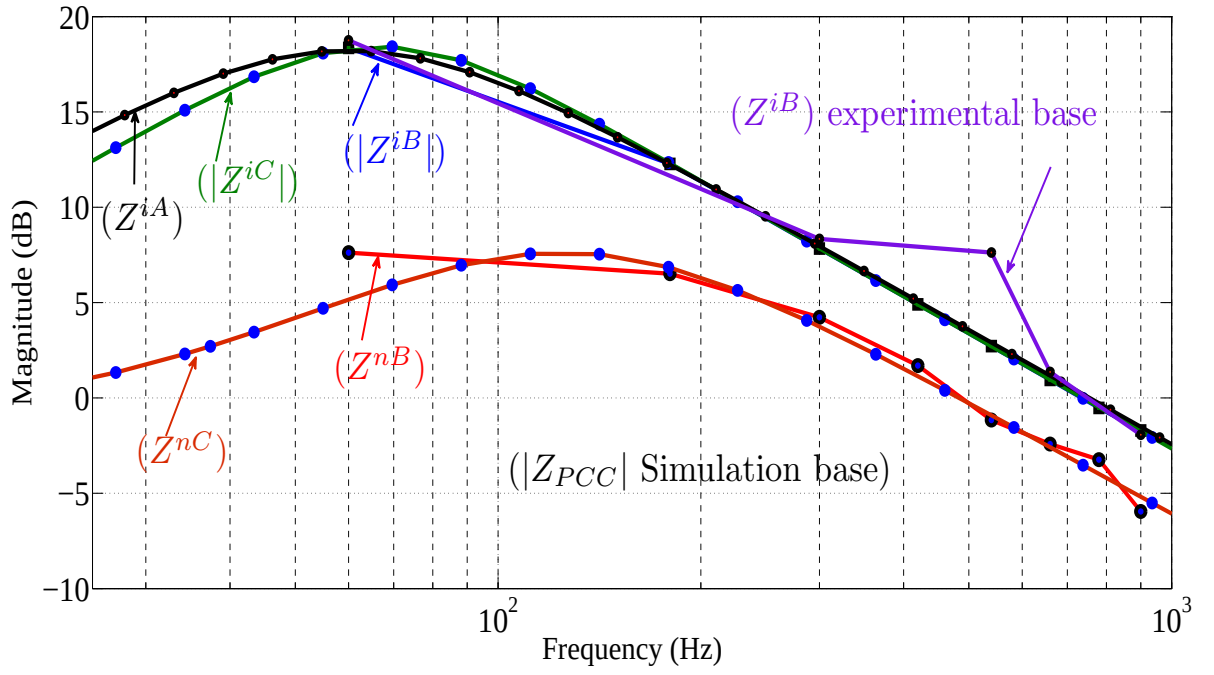


Fig. 3.8: Impedance at the PCC based on simulation tests.

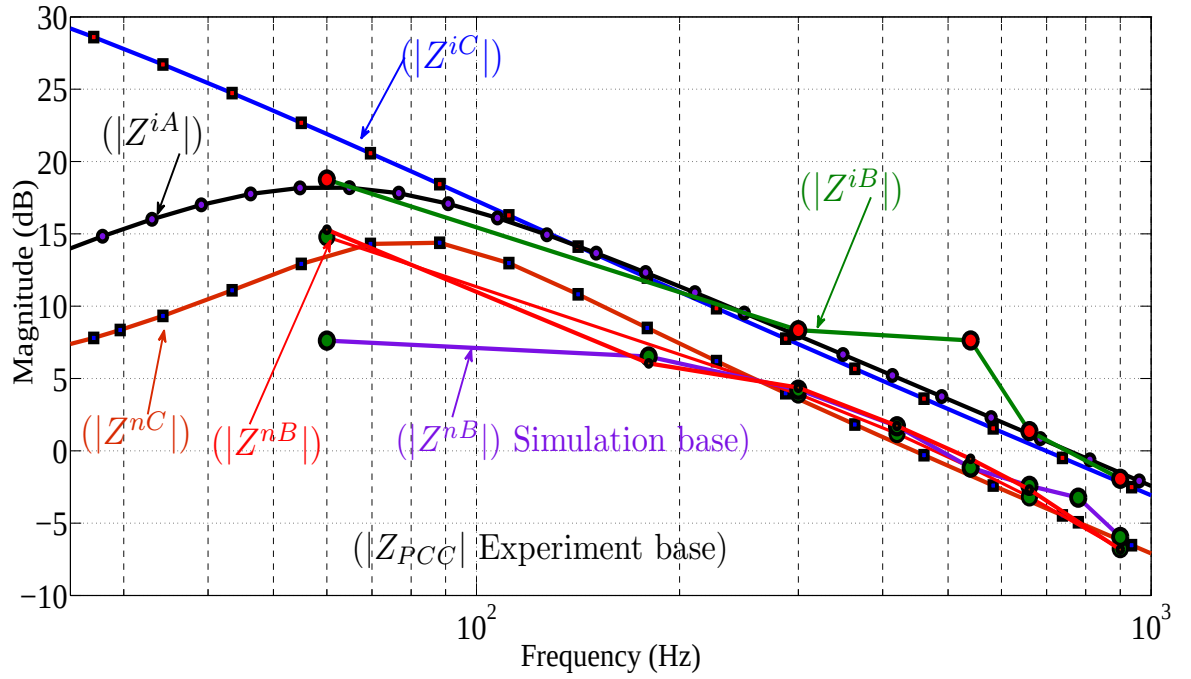


Fig. 3.9: Impedance at the PCC based on experimental tests.

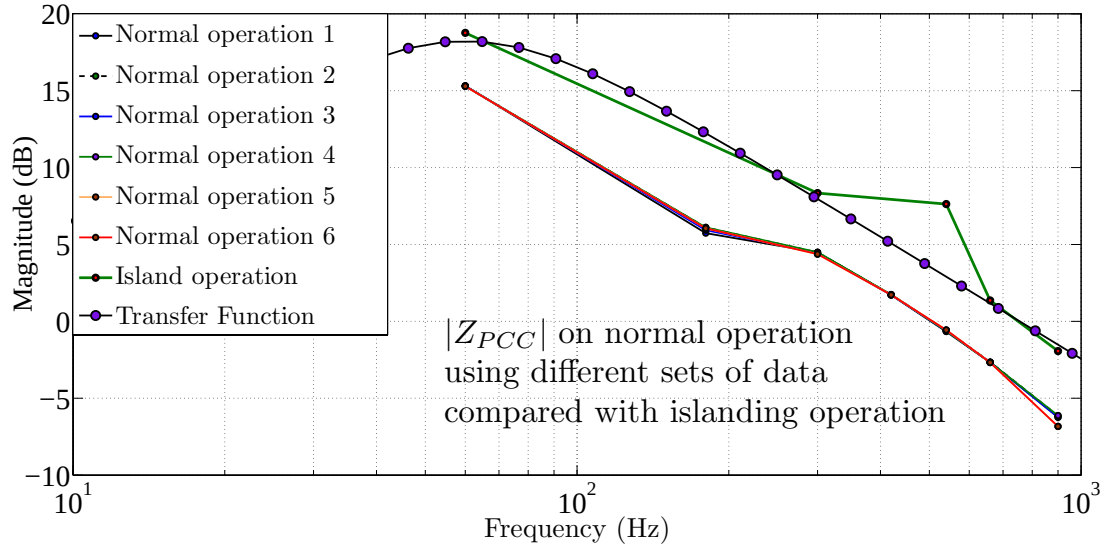


Fig. 3.10: A superimposition of the $|Z_{PCC}|$ based on experimental tests using different sets of data.

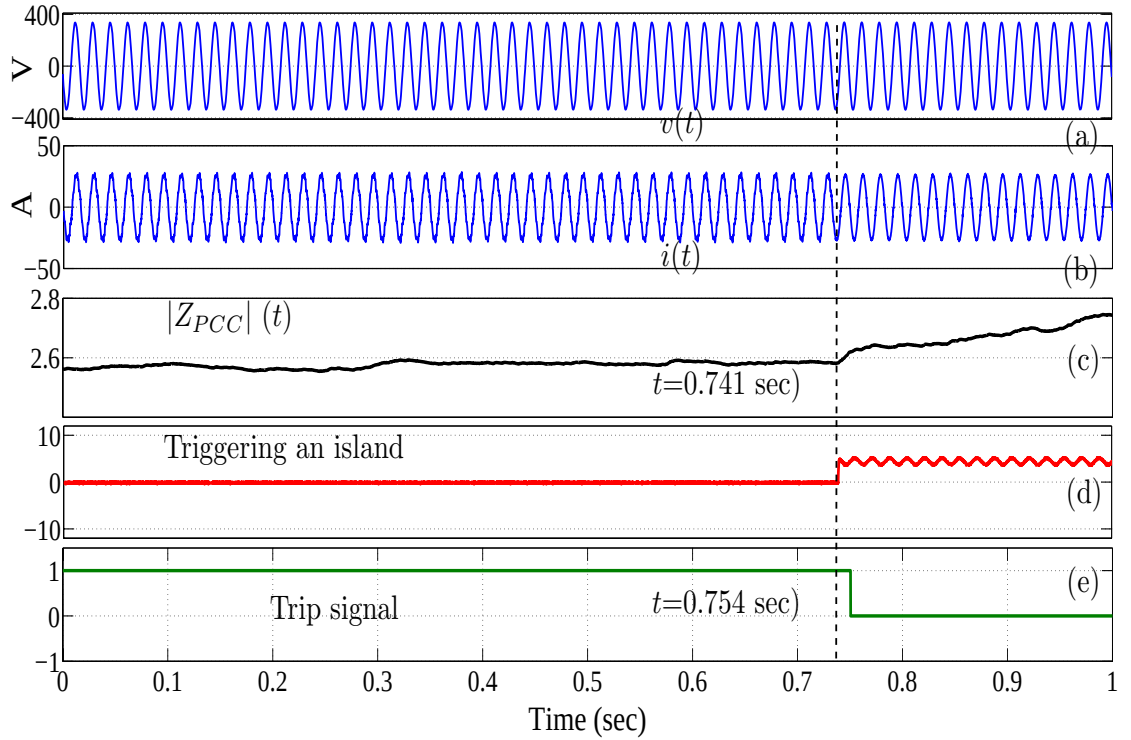


Fig. 3.11: The FDI algorithm response along with the voltage and current at the PCC.

The $|Z_{PCC}|$ was computed using three different techniques to establish the validity of the electrical circuit model and develop the impedance based technique for islanding detection. The results were superimposed, as shown in Fig. 3.8, Fig. 3.9, and Fig. 3.10. The impedance versus frequency at odd frequencies, $\omega \in [\omega_r]$, ($r = \text{odd harmonics} = 1-15$), in both normal operation and islanding operation, was computed based on simulation data, as shown in Fig. 3.8. $|Z^{nB}|$ and $|Z^{iB}|$ were the impedance magnitude at the PCC, computed using a ZFT for normal and islanding operation, respectively. $|Z^{nC}|$ and $|Z^{iC}|$ were the impedance magnitude at the PCC computed using ZLS for normal and islanding operation, respectively. In addition, $|Z^{iA}|$ was the impedance magnitude computed using the ZTF along with $|Z^{iB}|$, which is $|Z_{PCC}|$ computed using the ZFT technique for the experimental data. The results validated the possibility of computing the impedance as a continuous function of frequency by fitting the selected points to a transfer function model of the impedance. For the sake of validity, Fig 3.9 shows the superimposed results of the computed impedance based on the experimental data compared to the parametric calculated impedance, where it showed that the $|Z_{PCC}|$ over a range of frequencies showed a agreement for both simulation and experiment data along with the parametric model. The results demonstrated that over the odd frequencies, $\omega \in [\omega_k]$, where the region of $|Z^{nB}|(j\omega)$ and the region of $|Z^{iB}|(j\omega)$ at the same selected frequencies had sufficient separation, where it was possible to distinguish between two impedances and be able to compute the threshold. Also, this distinction was feasible at the fundamental frequency, where it was difficult to extract any feature using the existing passive methods. The results in Fig. 3.11 illustrate the ability of the introduced methodology to detect and respond to the islanding operation under the conditions that were listed in section 3.5.

Fig. 3.11(a) and Fig. 3.11(b) represent the continuous measurements of the voltage, $v(t)$, and the current, $i(t)$, at the PCC. Fig. 3.11(d) shows the recorded signal of the CB behaviour during normal and islanding operations. The island was created

at time ($t = 0.741$ sec). Fig. 3.11 (c) shows the $|Z_{PCC}|(t)$ before and after islanding, and Fig. 3.11(e) shows the trip signal of the ZFT response at time ($t = 0.754$ sec).

It can be concluded that the simulated and experimental along with the analytical results show good agreement. This agreement demonstrates the feasibility of the introduced methodology. The impedance based calculation using the simulated and experimental measurements for both normal and islanding operation compared with the impedance derived from the electrical circuit topology are demonstrated. The results demonstrate that it is possible to detect the island in the space where existing methods fail. These demonstrations confirm that a metric of impedance at selected frequencies can be used as a basis to distinguish islanding operation at those frequencies where there is no overlap between the region of normal and islanding operation. Furthermore, the results show that the measurements of voltage and current at the PCC are analytically linked to the impedance model, as seen by the DG at the PCC.

3.6 Specifying the Non Detection Zone (NDZ)

In order to completely characterize the ZFT-based anti-islanding protection, simulation tests were conducted in order to investigate the NDZ, and are compared with the NDZ presented in [7,26]. The simulation tests were performed for the initial power of the system as shown in Fig. 1.1 and described in section 3.2. The simulation model was created to match the same test bed inside the lab with the same grid impedance that had been estimated from the real tests. The objective of these simulation tests was to specify the NDZ for the presented method under the same conditions described in section 3.5, with the varied grid frequency in steps of 0.01 Hz up and down from $60\text{Hz} \pm 0.1\text{Hz}$, where $f = \pm \Delta f$ for both normal and islanding cases. The IEEE 1547 standard ranges of OF/UF relays were considered in all simulation tests. As seen in Fig. 3.13, the NDZ of UF/OF in contrast to that shown in Fig. 3.12 includes a DZ,

which means an improvement of 10% compared to the NZD of OF/UF.

3.7 Performance Comparison

Overall, the introduced FDI-based index has been compared with the reactive power based index, RPI, for passive islanding detection; it has been shown that FDI-based index is extracted based on the change of the system topology over a multiple frequencies, while the RPI is based on AC circuit analysis at a single frequency. The inputs of the FDI-based index are the voltage and current measured at the PCC, while inputs of the RPI-based method are the computed of reactive power. The missed alarms rate of the FDI-based index have showed improvement in comparison with the high level of missed alarms rate of RPI-based index, which is governed by OF/UF, where the results demonstrated it is possible to detect the islanding in the operating space where the existing methods failed to detect it.

3.8 Summary

This chapter has established the development of the FDI concept that is based on the measurements of V_{PCC} and I_{PCC} . The effectiveness of the proposed method has been verified in simulation and experimental tests supported by an electrical circuit model that is used to derive a transfer function for the impedance at the PCC. Furthermore, it has been shown, it is possible that the FDI to be computed as a continuous function of frequency by fitting discrete points to a transfer function of impedance. The results show that voltage and current measurements at the PCC are analytically linked to the impedance based measurement as seen by the DG. Moreover, the results show that the FDI-based index can reliably detect the islanding operation at the resonant frequency, and the simulation assessment has shown improvement by 10% compared to OF/UF. The effectiveness of the proposed techniques is verified in

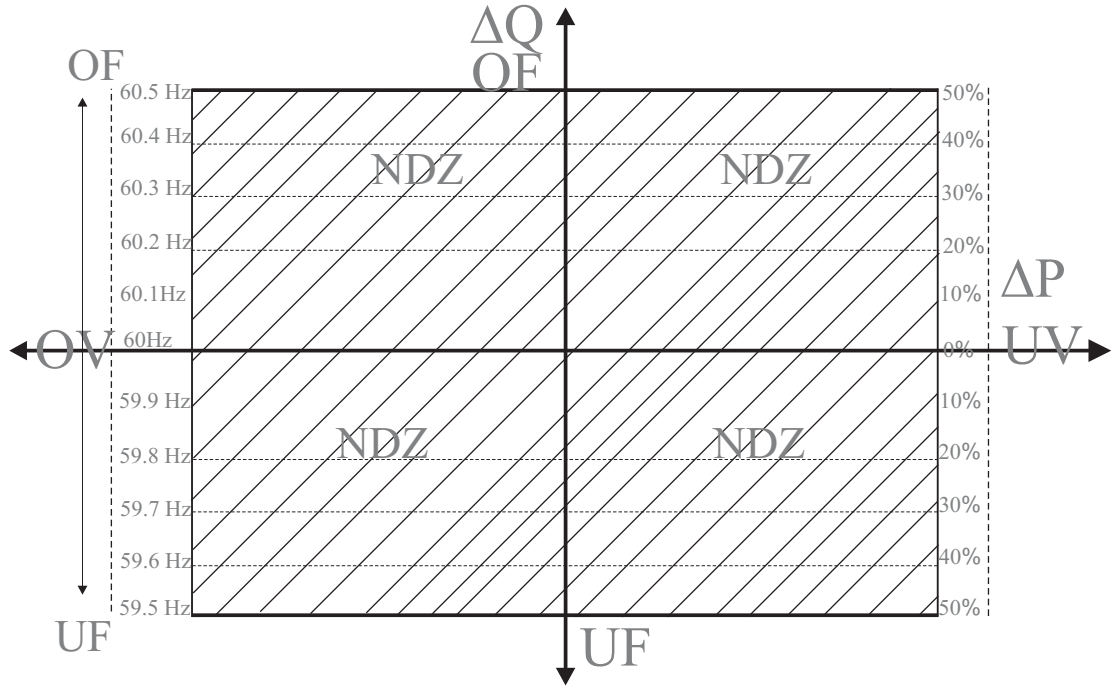


Fig. 3.12: NDZ of ΔP vs ΔQ for OF/UF.

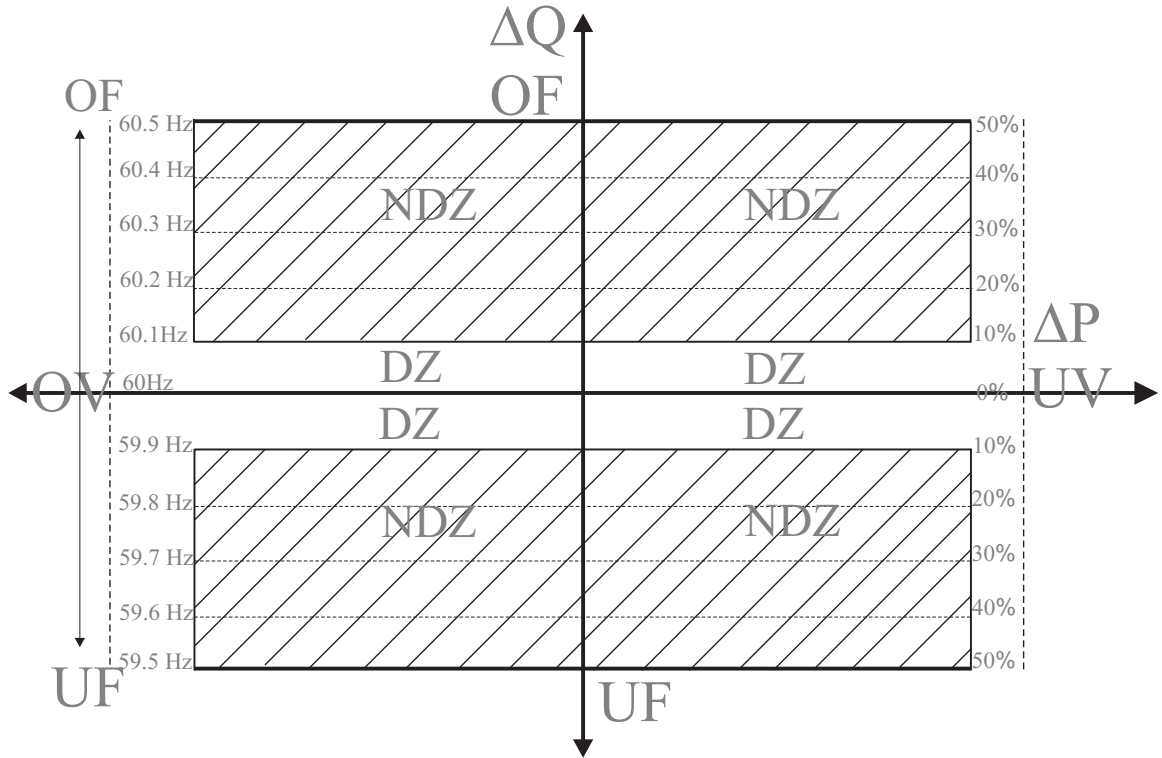


Fig. 3.13: NDZ mapping in ΔP vs ΔQ for the presented method compared with OF/UF.

simulation and experimental setups.

The contribution to the research presented within this chapter includes establishing a means of validating the experimental results of the theoretical analysis of impedance as an index for passive islanding detection. Furthermore, it demonstrated the viability of the electrical circuit model to characterize the change of interconnection topology. Moreover, the methodology shows an analytical link of the voltage and current at the PCC to the impedance model as seen by the DG at the PCC. Besides, the results confirm that although the impedance may be computed at a discrete point, it may also be computed as a continuous function of frequency by fitting the discrete points to the transfer function model of the impedance using simulated and experimental measurements. Nevertheless, the methodology possesses a detection zone, DZ, within the NDZ of the typical OV/UV and OF/UF protection relays.

Chapter 4

Online Testing of VPS Index

4.1 Introduction

This chapter presents the implementation and testing of a new anti-islanding algorithm that is based on the variation of signal energy over a certain band of frequencies contained within a virtual power signal (VPS). The VPS is obtained from the measurements of voltage and current at the PCC. The algorithm is implemented independently of the EPCs. The algorithm and the designed hardware are termed an independent anti-islanding relay, IAR. The new IAR may be attached at the PCC between DGs and the EPS. The advantage of such a design is that it may support integrating any DG to the EPS, which means it may be used for DG systems with EPCs or without, as well as for single-phase or three-phase systems. This chapter explains i) the selection and the process of the index used for detection, ii) design and development of the system platform, iii) implementation of the algorithm in a single-phase system including the hardware and software, and iv) evaluation of the performance through simulation and experimental testing.

4.2 The VPS Based Algorithm

The essence of the algorithm is based on monitoring the variation of certain harmonics contained in the virtual power signal over a certain time interval. This can be accomplished by computing a feature that reflects the variation in the third harmonic over a time interval using the FFT by transforming the measured PCC voltage and current. The selection of the third harmonic is not limited and the algorithm may employed multiple harmonics. The third harmonic is selected due to the fact that it is the dominant harmonic in a single phase system [63]. Islanding detection is based on the calculated value of a non-negative index, $C(n)$. The index, $C(n)$, depends on the FFT of the measurements of the voltage and the FFT of measurements of the current at the PCC. The index is chosen such that during islanding the value of the index satisfies, $C(n) > b$, and during normal operation, $C(n) < a$. If under all operating conditions, $b > a$ then the detection of islanding will be 100% correct with zero false alarms and zero missed alarms if the threshold, β , is chosen such that $a < \beta < b$. In the event that $a > b$ then there is a risk of missed alarms and false alarms depending on the choice of the threshold. In this case, if $\beta \leq b$, then there will be zero missed alarms but there will be operating conditions during normal operation that will result in false alarms; if $\beta \geq a$ then there will be zero false alarms but there will be operating conditions during islanding operation that will result in missed alarms; if $a < \beta < b$ then there will be operating conditions during normal operation that will result in false alarms and missed alarms.

The algorithm is tested using simulation data records of voltage and current, and using actual experimental data. Then, the algorithm is implemented and tested online with a 7 kW current-controlled voltage-source inverter connected to the EPS. The presence of inherent harmonics in DG power converters and distribution systems is used as a basis of islanding detection. When an island occurs, the impedance at the PCC, as seen by the DG, increases suddenly, as described by equations (2.1) and (2.2)

and in transfer function form as in equations (2.4) and (2.6). A change in impedance results in a sudden increase in the third harmonic of the PCC voltage and current, and this serves as the basis for islanding detection. The variation of signal energy over a certain band of frequencies contained within a virtual power signal, VPS, is the basis of this method. The mathematical derivation of the algorithm is explored by considering a uniformly sampled signal, $x(m)$, with an implied sample period, h . The associated FFT can be expressed as

$$X(n, k) = X(n, \omega) \mid \omega = \frac{2\pi}{N}k \quad (4.1)$$

Equation (4.1) can be manipulated as follows:

$$X(n, k) = \sum_{m=-\infty}^{\infty} x(m) w(n-m) \exp(\lambda) \quad (4.2)$$

where $\lambda = (-j\frac{2\pi}{N}k)$, $w(n)$ denotes a window that is unity over $[0, N-1]$, $X(n, k)$ is the transformed signal associated with window n , and the frequency as $2\pi k/Nh$. Given a measurement record, m , consisting of N samples of $v(t)$ and $i(t)$, sampled uniformly over period, h , the associated FFT's, $V(n, k)$, $I(n, k)$, and $\phi(n, k)$, are then used to generate an intermediate classification feature. $F(n)$, the feature associated with record n , can be defined as in equation (4.3).

$$F(n) = \sum_{\text{Selected } k} E(n, k) \quad (4.3)$$

where

$$E(n, k) = V(n, k)I(n, k) \sin(\phi(n, k)) \quad (4.4)$$

$F(n)$ represents a metric of $E(n, k)$ over a selected band of frequencies. In consider-

ation, the detrended series is formulated as

$$f(n) = \left\{ \tilde{F}(n), \tilde{F}(n-1), \dots, \tilde{F}(n-N+1) \right\} \quad (4.5)$$

$$\tilde{F}(i) = F(i) - \frac{1}{N} \sum_{j=n}^{n-N+1} F(j), \quad i = n, n-1, \dots, n-N+1 \quad (4.6)$$

The series, $f(n)$, represents the variation in $F(n)$ about its mean value over a time interval of the most recent N records. The mean is removed to increase the numerical resolution of the FFT computation. The signal energy in the series, $f(n)$, is given by

$$\mathfrak{S}(n) = \frac{1}{N} \sum_{k=0}^{N-1} |X(e^{j\omega})|^2, \quad \omega = \frac{2\pi}{N}k \quad (4.7)$$

Here, X represents the FFT coefficients of $f(n)$ [56]. $\mathfrak{S}(n)$ represents the size of the variation in F over the most recent N records. The islanding classification index, $C(n)$, is defined as a measure of the change as expressed by

$$C(n) = |\mathfrak{S}(n) - \mathfrak{S}(n-1)|/T \quad (4.8)$$

where $T = Nh$ is the time interval between successive records. $C(n)$ is a measure of the difference in signal energy over a time interval of Nh . Islanding is detected when the magnitude of $C(n)$ exceeds preset threshold limits. During implementation, the threshold is chosen to be small enough in order to eliminate missed alarms and large enough in order to eliminate false alarms. The anti-islanding algorithm is implemented within the TMS320F28335 floating point DSP. The flow chart of the sequence of steps to extract the VPS feature is shown in Fig. 4.1. The mean of the collected data of the samples ($n=64$) are in the sliding window. The DC trend is removed to eliminate and increase the numerical resolution of FFT computation. The variables $v(t)$ and $i(t)$ are the monitoring voltage and current at the PCC. Monitoring

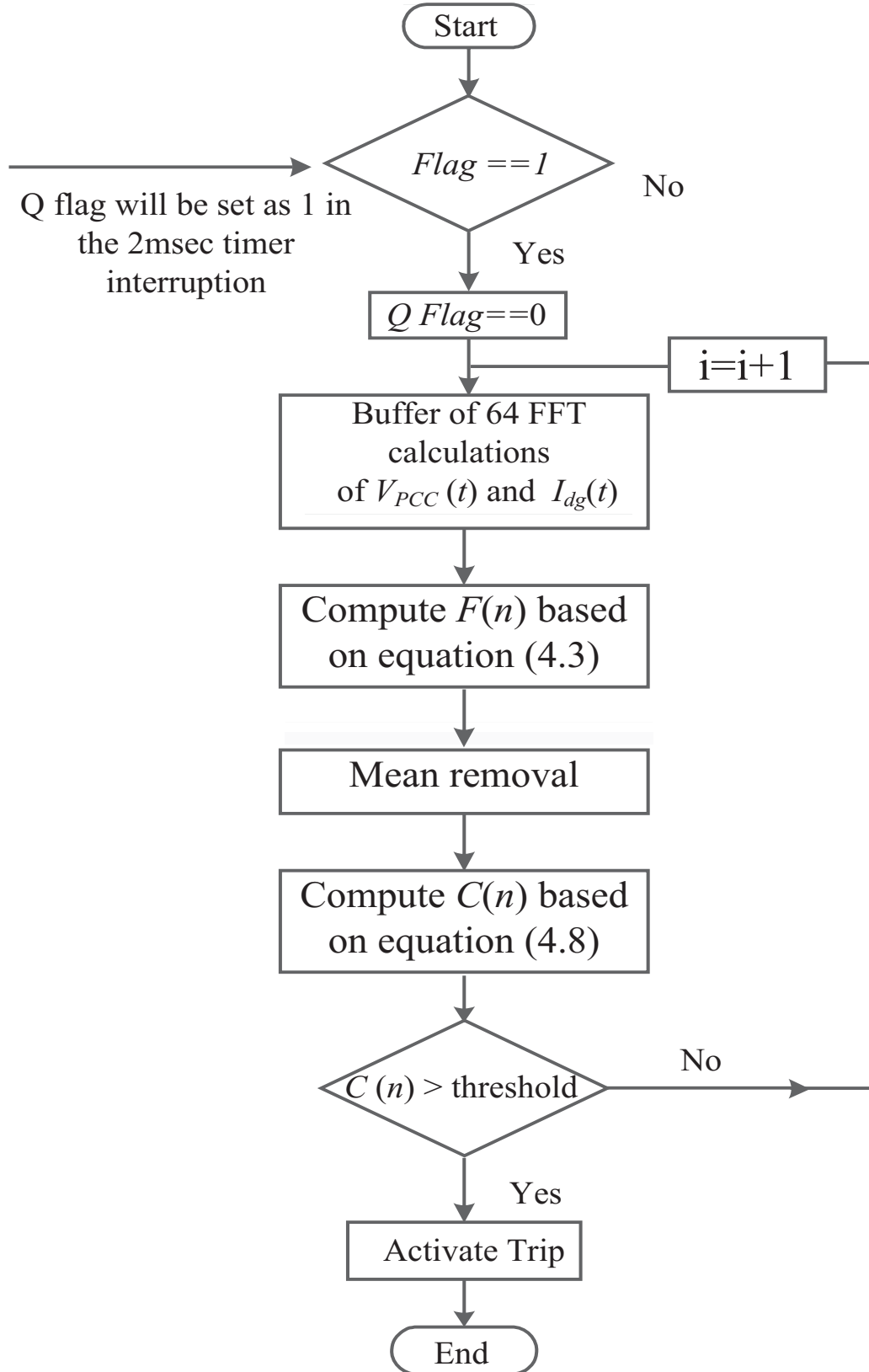


Fig. 4.1: Flow diagram depicting passive anti-islanding algorithm objective function.

variables are sampled into a buffer size of 64 points, and the timer was used to trigger the computation of $F(n)$ at an interval of 2 msec.

4.3 Development of Hardware Platform

The schematic of the IAR with the system topology that is employed to examine islanding appears in Fig. 4.2. The manifestation of IAR is designed and constructed for a laboratory test system. The constructed design consists of the input power for grid side, EPSa, EPSb, and EPSc protected with fuses (F), voltage divider (VDR), and the input power from the inverter side, INVa, INVb, and INVC, with required fuses, power board, interface board and DSP board, and contactors, C1 and C2. The power board includes voltage and current sensors that monitor the voltage and current, Ia, Ib, Ic, Vab, Vbc, and Vca, and provides the data input to the interface board. The interface board provides all required signals and energizes the DSP board, and it consists of the hardware protection relays, analog filters, LCD that displays the states of the IAR, the input and output signals, and the power supply for the DSP board. The DSP board includes a TMS320F28335 and a chip from Texas Instruments, with a 32-bit floating point TMS320F28335. The Implementation code is written in assembly and C languages. The code is designed and written to be modular and reusable, so that the chip used in IAR may be reprogrammed for any further algorithms. Fig. 4.3 shows the physical component of IAR developed and constructed to conduct online tests as part of this dissertation. The IAR platform is designed in such a way that allows for developing new anti-islanding schemes, and it may be packaged and commercialized, where the design features of DSP allow for implementation and provide the flexibility to adapt any further suitable algorithms.

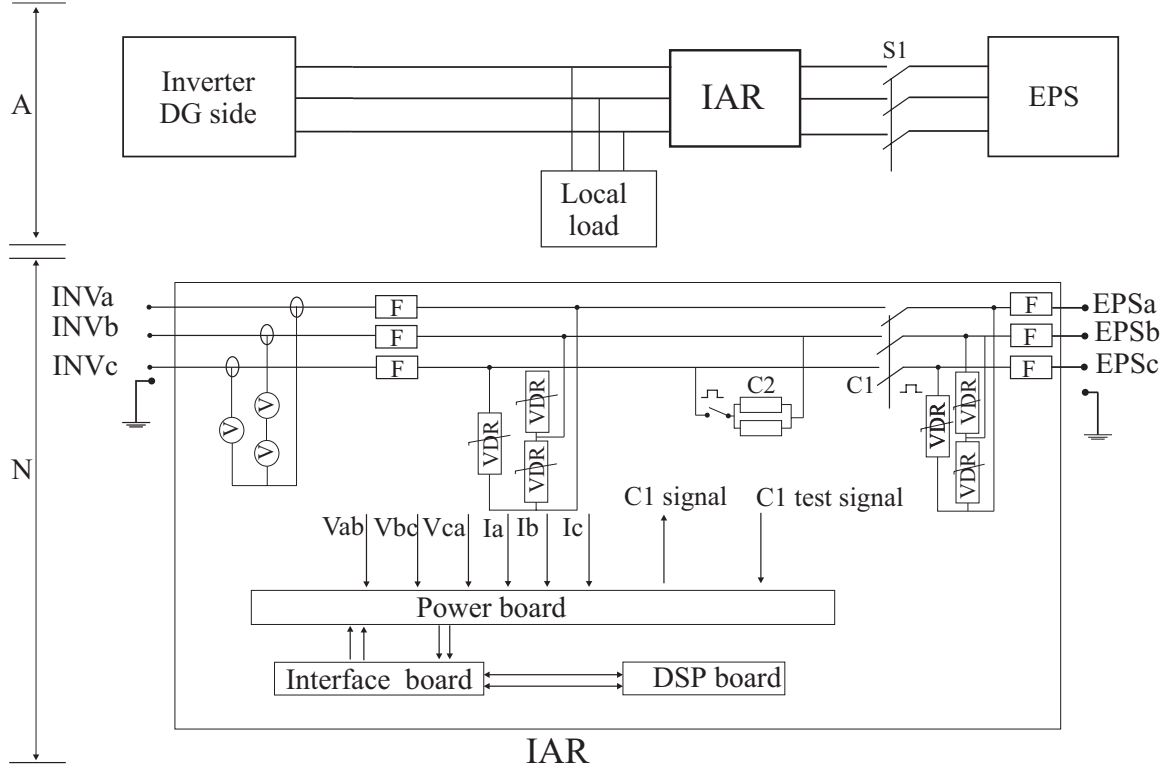


Fig. 4.2: A diagram of the architecture of the IAR with typical DG topology.

4.4 Systems Configurations

4.4.1 Simulation System

The MATLAB/SIMULINK SimPower Systems and Control Systems tool box was used to implement the simulation system shown in Fig. 4.5 that reflects the physical system shown in Fig. 1.1. The DG uses a three phase power supply from the SimPower Systems tool box. The single-phase inverter was modeled as an AC-DC-AC converter, together with a rectifier, boost chopper, and single phase inverter, with filter characterized by L_F , C_F , R_F , and the required control circuit. The control circuit of the inverter and its specification are shown in Fig. A.1 and Table A.1, respectively. The local load was modeled as a parallel RLC load. The EPS was modeled as

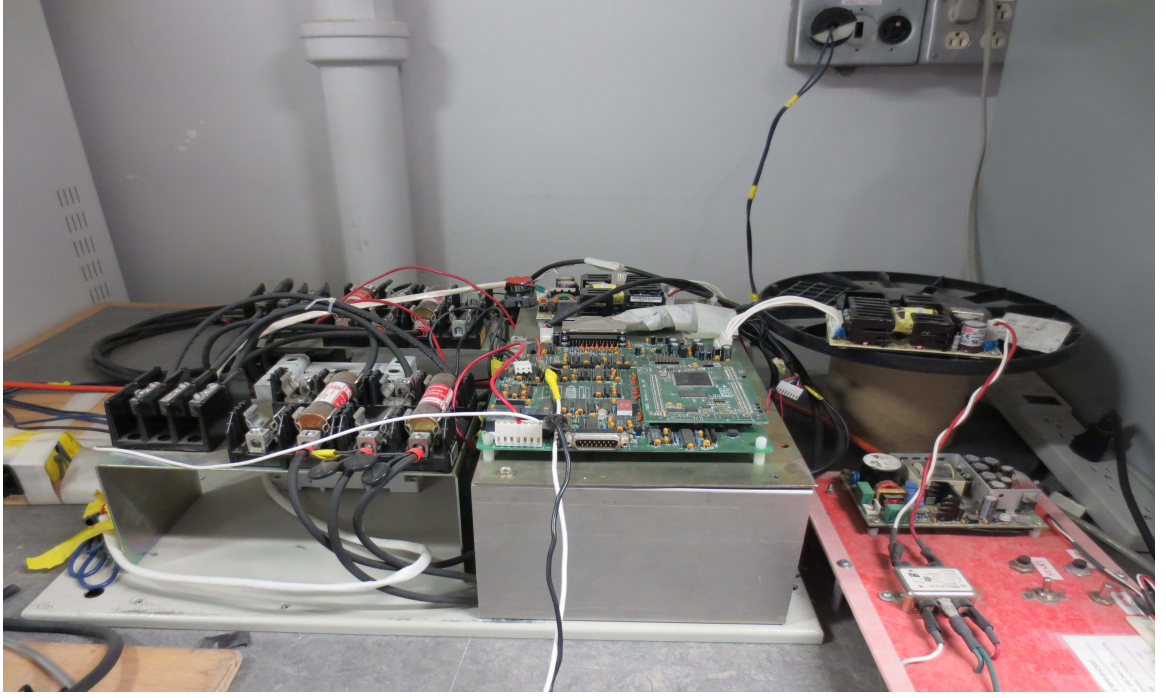


Fig. 4.3: The hardware of the IAR designed and constructed for online tests.

a single-phase voltage source with an equivalent grid impedance, $Z_{EPS} = R_g + sL_g$. The system parameters used for the simulation are provided in Table. 4.1.

Table 4.1: Simulation System Parameters

R_g	$6 \times 10^{-6} \Omega$
L_g	$2 \times 10^{-6} H$
Rated power	7 kW
Restive load	8.3Ω
Captive load	$353 \mu F$
Inductive load	18.3 mH
Inverter output	30 A

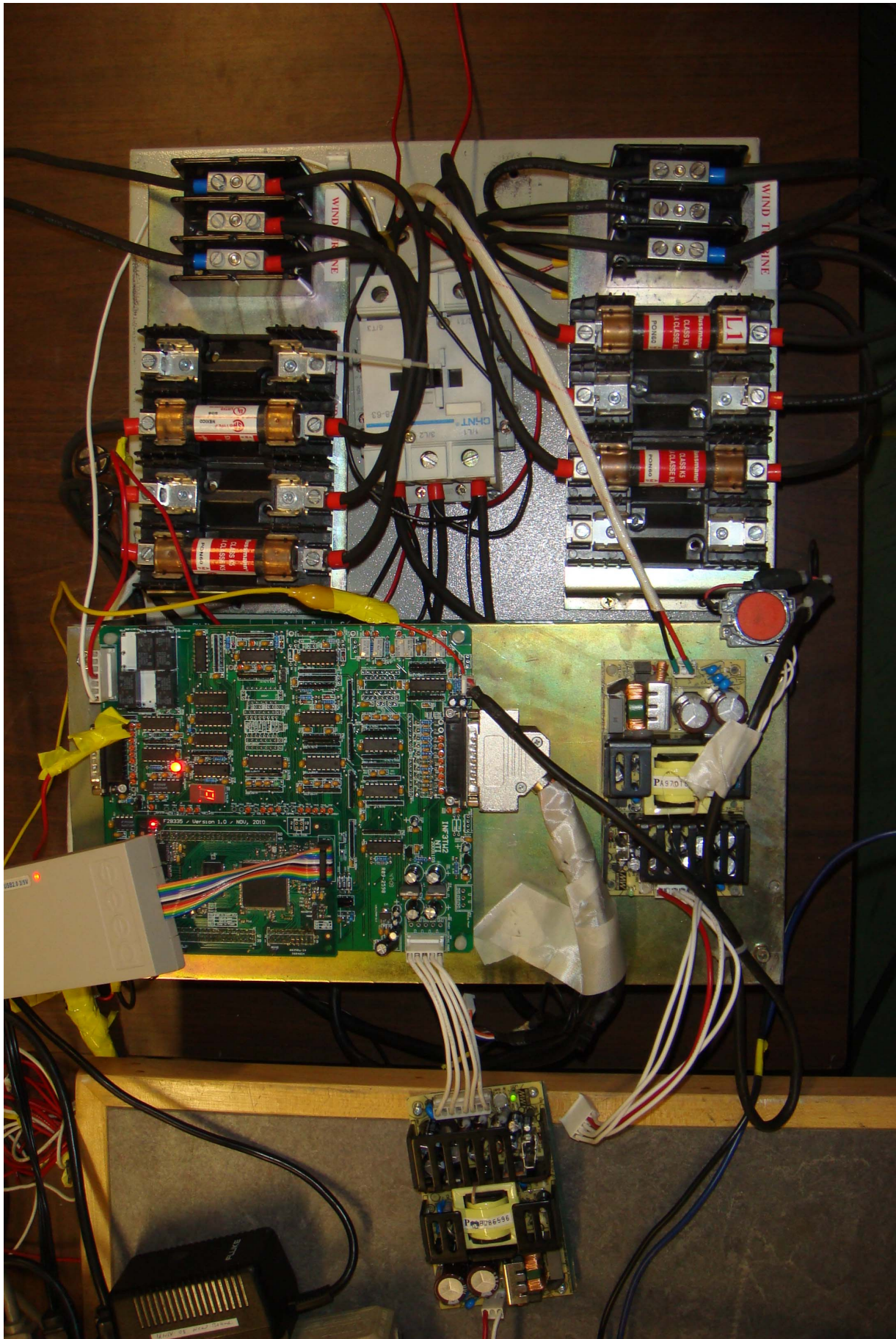


Fig. 4.4: The anti-island relay designed and constructed for this thesis in the sustainable power lab.

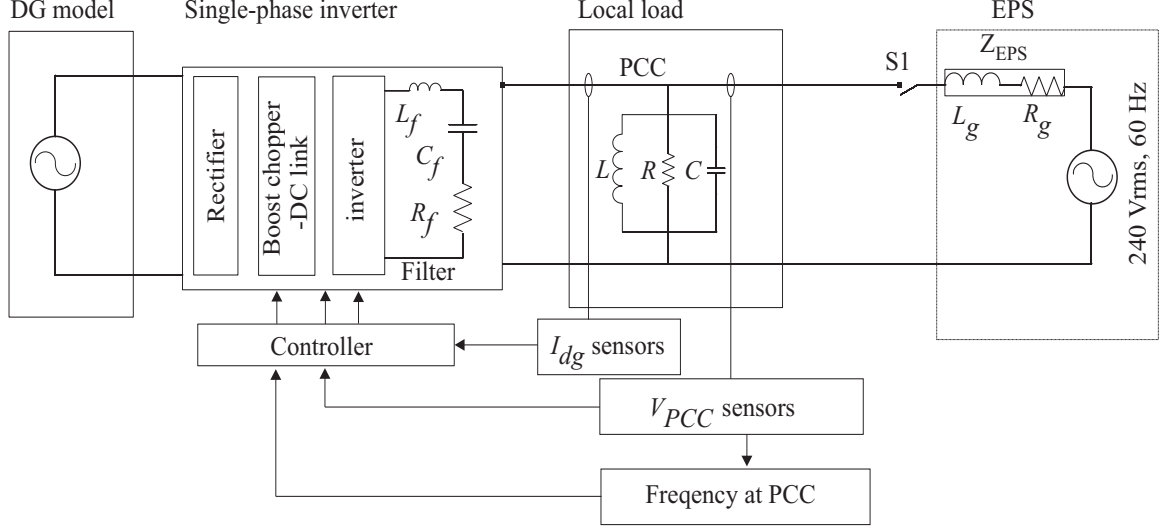


Fig. 4.5: Single-line diagram of the simulation system.

4.4.2 Experimental Test Systems

The system in Fig. 1.1 is represented by the experimental test bed shown in Fig. 4.2. The 240 V/50 A power supply connected into a model-I 12-60 12 kW single-phase inverter that is connected to 240/60 Hz EPS at the PCC. The local load was a parallel of resistive, capacitive and inductive load. The system is constructed with designed physical hardware of IAR, as shown in Fig. 4.1. A circuit breaker, 240 V/50 A, was used to create islanding. Sensors for voltage and current are used in the schematic diagram of the experimental test bed shown in Fig. 4.2. Fig. 4.6 and Fig. 4.7 show photographs of the experimental setup for the 7 kW DG-EPS system used for implementation and assessment tests for presented algorithm. The system parameters are provided in Table 4.2.

Table 4.2: Experimental System Parameters

Grid voltage (V_{grid})	240 V
Grid frequency (f_{grid})	60 Hz
Output inverter power	7 kW
Inverter filter	
L_f	0.01 mH
R_f	0.01 Ω
Local load	
R	8.3 Ω
C	353 μf
L	9 mH

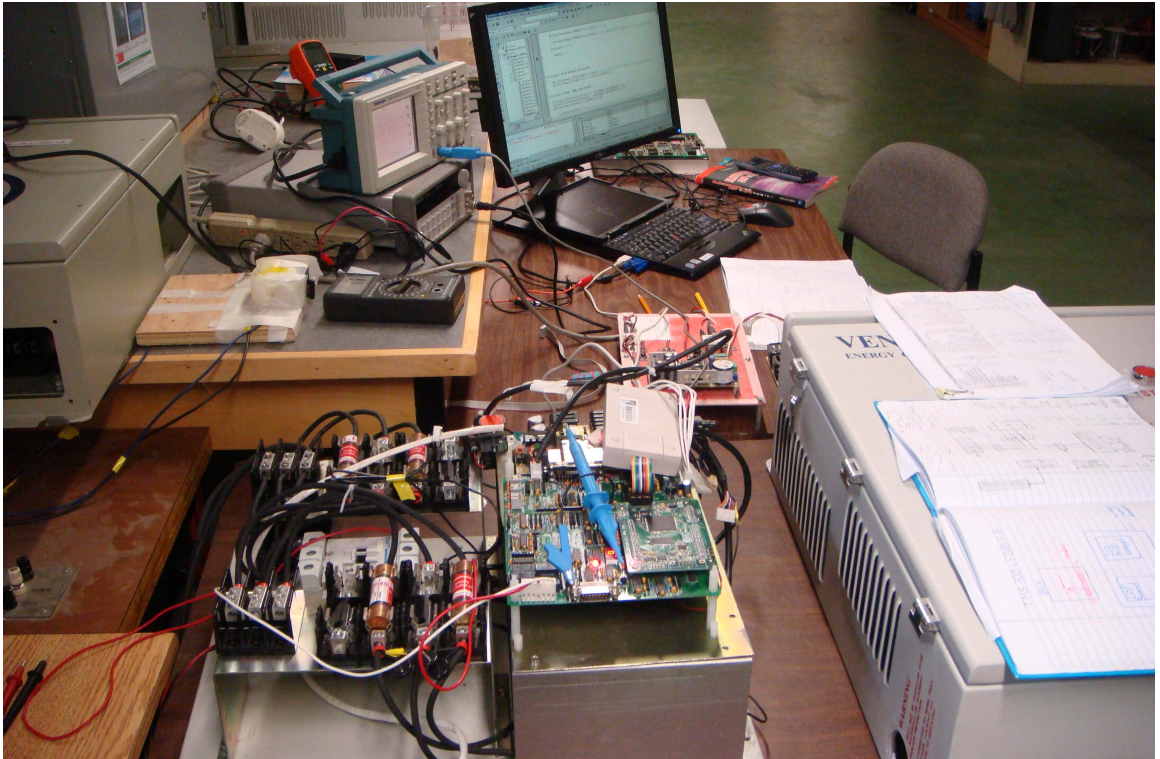


Fig. 4.6: A photograph of the experimental setup.



Fig. 4.7: A photograph of the experimental setup.

4.5 Simulation and Experimental validation

4.5.1 Simulation validation

The computer simulations were conducted to verify the feasibility of the algorithm and to test the index as well as to perform a comparative analysis with the existing detection schemes. The system is simulated in different modes in order to investigate the values of $E(n, k)$ for $k = 1, 2, 3$, and 4 during an islanding event. The simulation test confirmed that the magnitude of $E(n, 1)$ is very small and the variation in $E(n, 3)$ increases significantly during an islanding operation.

4.5.2 Experimental validation

Different scenarios for data collection were conducted in order to test the algorithm off-line. The algorithm is embedded into the IAR, where the TMS320F28335, DSP

takes place, as shown in Fig.4.6 and Fig. 4.7. The tests were conducted at the rated power of a 7 kW inverter and local load, and the system parameters were as shown in Table. 4.2. For this experimental step, the grid voltage was 240 V at a frequency of 60 Hz, and the output from the inverter was 30 A. The main focus is on the scenario of the balanced power between the DG and local load, in which ΔP and ΔQ are close to zero. As can be seen from Fig. 4.8 [64], the experimental data records of the DG voltage, $v(t)$, current, $i(t)$, and the breaker position collected just after the islanding event. The cumulative time for recording data is 0.4 sec. The islanding event occurred at time instant, 0.1964 sec.

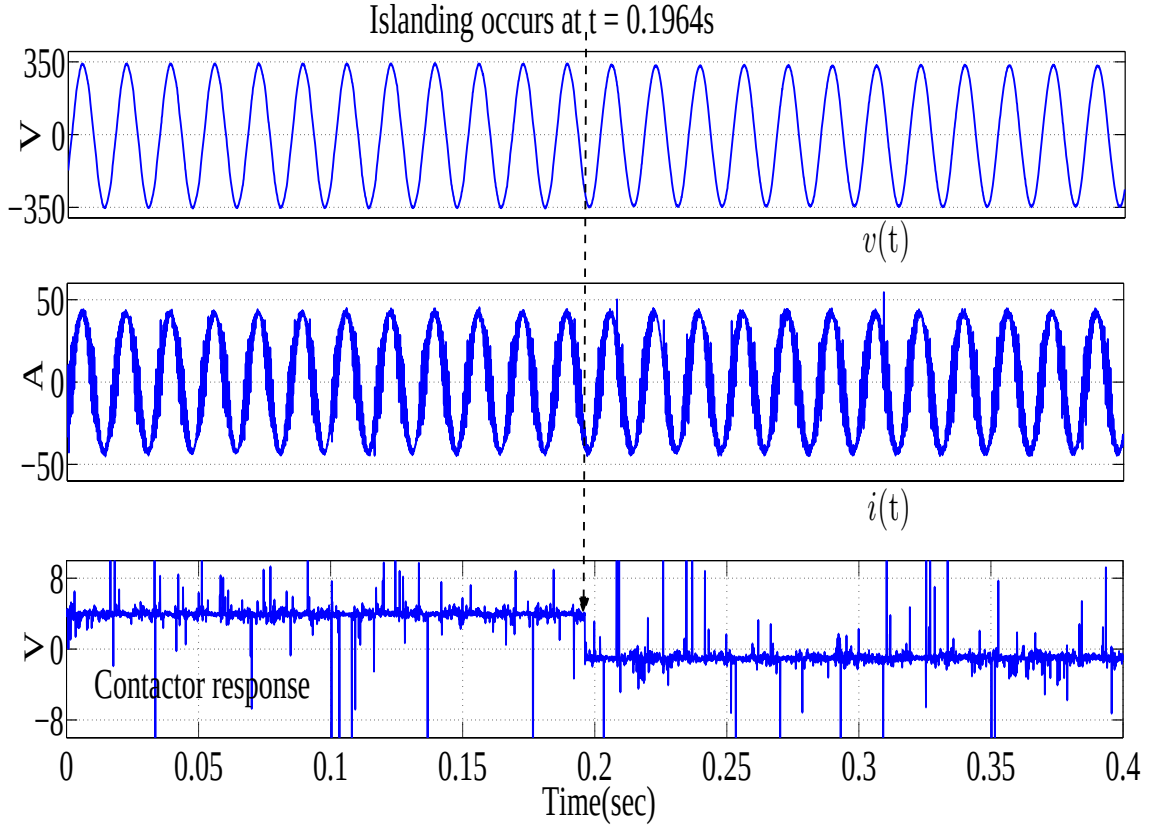


Fig. 4.8: Real time measurements of voltage and current along with contactors response in the case of island at the PCC.

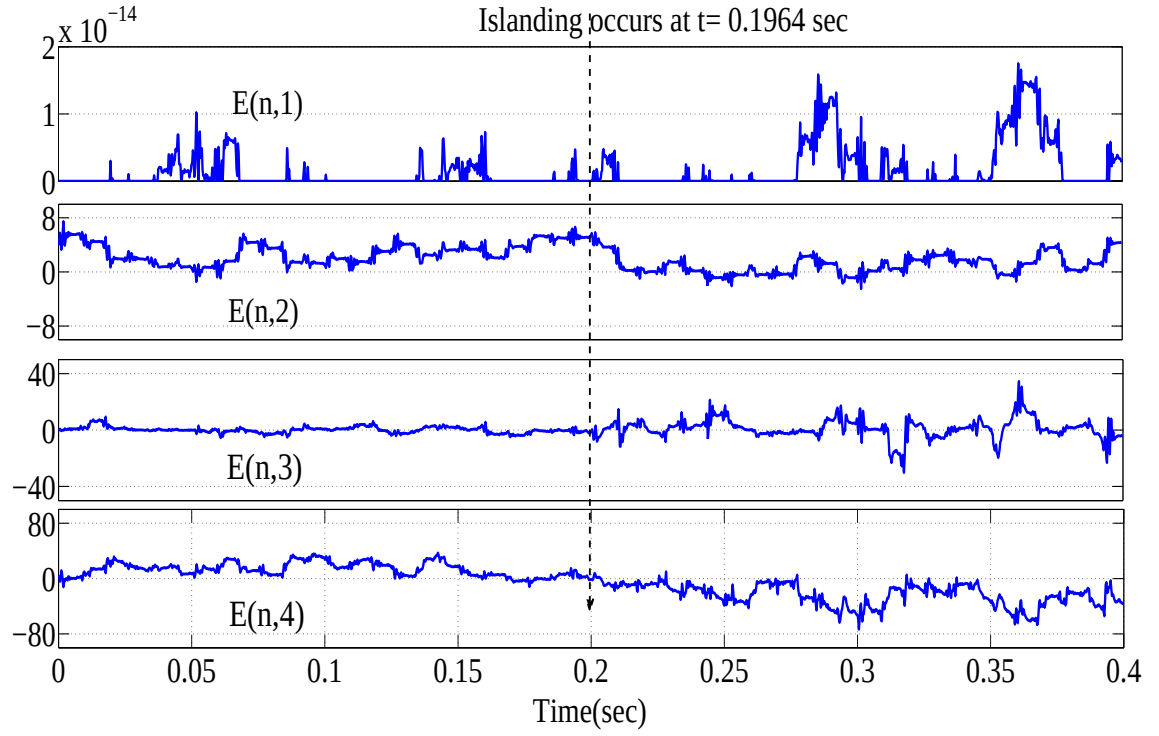


Fig. 4.9: The magnitude of $E(n,k)$ based on experimental testing.

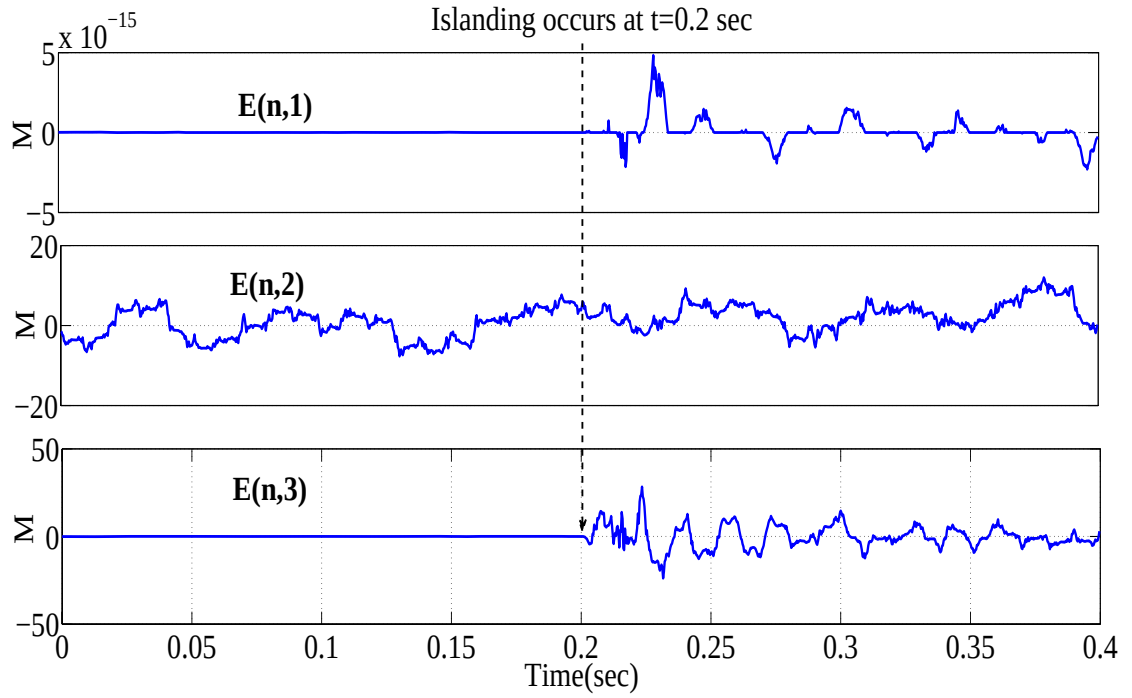


Fig. 4.10: The magnitude of $E(n,k)$ based on simulation.

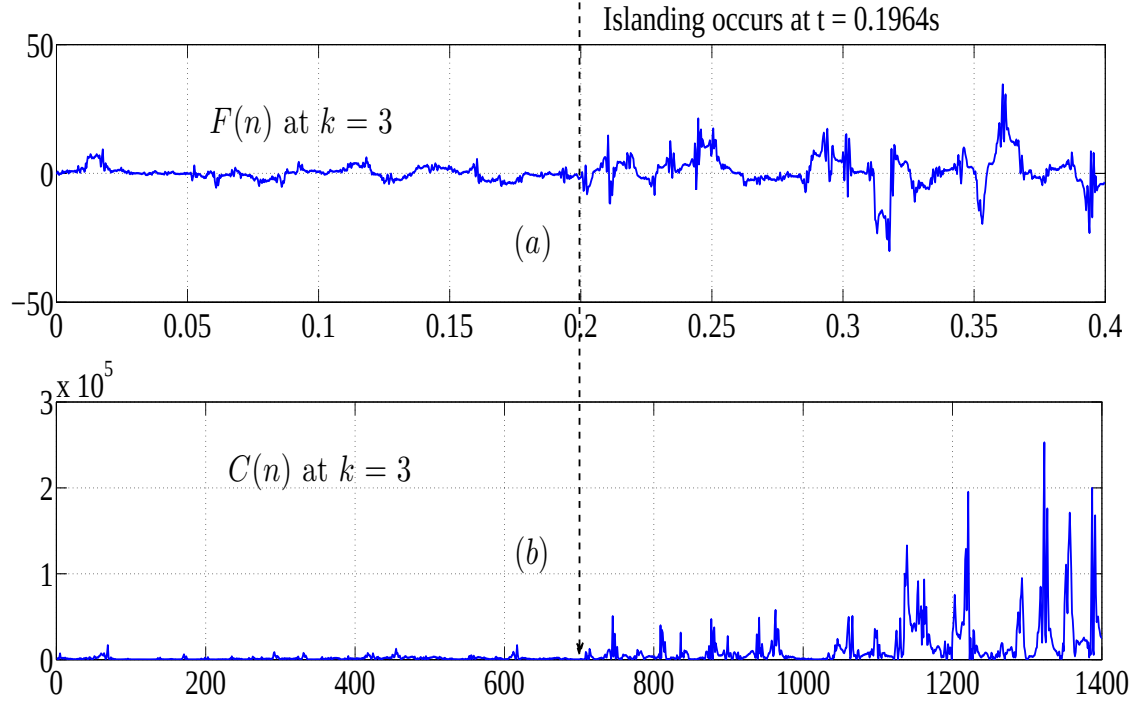


Fig. 4.11: The magnitude of $E(n,3)$ and $C(n)$ based on experimental tests.

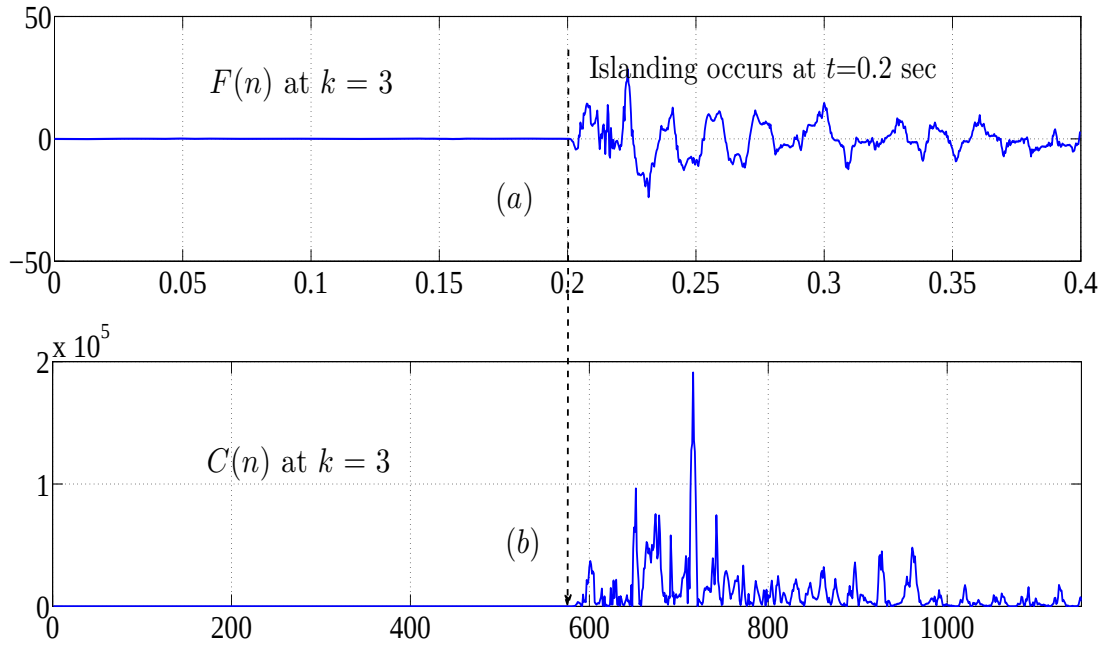


Fig. 4.12: The magnitude of $F(n)$ and $C(n)$, $k=3$ based on simulation.

Fig. 4.9 and Fig. 4.10 demonstrate simulation and experimental results at distinct values of energy at different orders of harmonics. These results showed consistency at the same point. Fig. 4.9 shows the computed values of the 1st through 4th harmonics of $E(n, k)$ using the simulation data. The magnitude of $E(n,1)$ is too small to be considered for islanding detection. $E(n,2)$ and $E(n,4)$ show an apparent reduction in magnitude after the islanding event has occurred. However, the trend in $E(n,2)$ and $E(n, 4)$ was not significantly different between grid-connected and islanding conditions. For $E(n, 3)$, there was a marked change in both magnitude and rate of change following the islanding event. Consequently, $E(n,3)$ was chosen as the signature for islanding detection. The corresponding plots of $E(n,3)$ and $C(n)$ experimental data are in Fig. 4.11 and Fig. 4.12. Those figures show that islanding may be detected with a suitable choice of threshold.

4.5.3 Detection Time

The detection time is the duration between the interruption of the utility and the tripping of the circuit breaker to disconnect the DG. In this technique, the current perturbation is introduced every 20 cycles. As a result, when a worst case scenario occurs, islanding was formed at the end of the perturbation period and the maximum detection time is 330 msec, which was less than the 2 sec limit specified by the IEEE standard 1547.1. This maximum detection time was also valid for different loading conditions. Fig.4.13 illustrates the voltage and current waveforms along with the trigger signal, which confirmed that the islanding operation occurred at 0.13 sec and was cleared at 0.46 sec. The results demonstrate that the algorithm is very effective. The time clearance remained within time mandated by the standard.

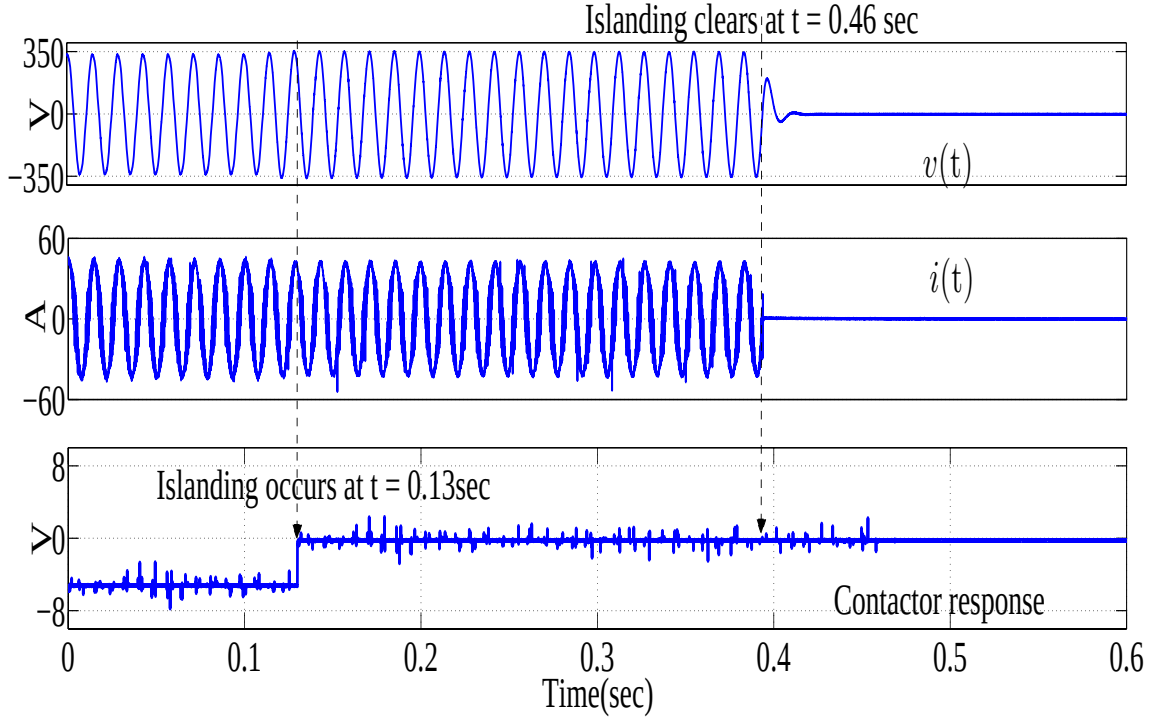


Fig. 4.13: The trip signal associated with the voltage and current at the PCC.

4.6 Discussion

In this chapter, the constructed system and employed software have been discussed. The proposed islanding algorithm uses the change in the computing of VPS at a specific harmonic, and it can be extended to be used at multiple harmonics. The virtual signal change at PCC is based on the change of the interconnection topology as seen by the DG side.

The hardware has been designed and tested, followed by algorithm implementation and testing for a 7 kW DG system. The technique has been verified in simulation, and validated in the prototype unit constructed and tested experimentally in the laboratory. The investigation and tests have been conducted for a single-phase inverter with a linear parallel RLC load. It may be concluded that the method consistently showed a change in third harmonic as the basis of islanding detection. The change

of the third-harmonic results from the change of the impedance at the PCC. This index is directly related to the impedance based detection methodology introduced in Chapter 2 and Chapter 3. Even though the index is different, the index is still related to the change of the interconnection topology.

4.7 Summary

This chapter discusses the implementation of the new index that is tested online. The technique used is based on monitoring the size of the variation of certain harmonics contained within the VSP over a specific time interval. Results show that for a very small DG, an island can be quickly detected. The feasibility and validity of the proposed algorithm are verified through simulation and experiment. The hardware development setup can be used to implement any index or multiple indices. The research contributions associated with this chapter include i) a new index is presented; ii) the IAR is designed, constructed, and tested online compared with [56] that shows the index is embedded within the PEC; and iii) the validity and performances assessment of the proposed algorithm is demonstrated in both simulation and online tests.

Chapter 5

Time Frequency Dependent Based Index

5.1 Introduction

The difference in the impedance measurement between islanding and normal operation may result in a small NDZ for radial systems with strong network connections. Several researcher used the impedance method to detect islanding; however, these methods used "Signal Injection" in an attempt to realize passive islanding detection methods such as in [34]. For example, the single non-harmonic frequency injection is found to be an effective impedance measurement method. However, the technique requires a high-cost interface to the power system. The technique introduced within this chapter is based on impedance measurements, where signals already present in the power network are used in order to minimize effects on the power quality.

This chapter focuses on an index based on a time frequency feature extracted using the WPT. The approach is a variation of that used in [9, 65] for islanding detection. The variation on the index is new to passive islanding detection schemes, and the index is computed based on the change of zero sequence impedance (ZSI). The ZSI

is founded upon the fact that a balanced three-phase system results in infinite zero sequence impedance (open circuit). However, in the case of islanding, those conditions are not valid any more; therefore, the ZSI may have abrupt changes in values that may be extracted and used as a basis for islanding detection. The ZSI is defined by the ratio of zero sequence voltage to the zero sequence current that originally transformed based on the measurement of voltage and current at the PCC.

The use of ZSI as anti-islanding index may offer some advantages over the existing schemes; it may be applicable in DG systems that use PECs as well as DG systems that are directly connected to the EPS. Furthermore, it is better than the impedance measurement techniques in [34,66] because it does not degrade power quality. Moreover, the ZSI is enhanced in terms of time response compared to standards, standard response time of 2 sec. The sensitivity of the new index has been assessed across a range of operating conditions using simulation data and in some cases records data collected from the laboratory test system.

5.2 System Test Configurations

5.2.1 Simulation Model

The MATLAB/SIMULINK SimPower Systems and Control Systems tool box were used to implement the simulation of a three-phase system (3ϕ) shown in Fig. 5.1 that reflects the physical system shown in Fig. 1.1. The DG was modeled as a wind turbine within a 10 kW power rating and was interfaced as the input to a 3ϕ inverter. The local load was modeled as a parallel RLC load. The EPS was modeled as a three-phase power supply interfaced to a power transformer with an equivalent grid impedance, $Z_{EPS} = R_g + sL_g$. The DG system was connected to the EPS at the PPC. The same system was modeled for simulation except the DG was replaced by a synchronous machine that was connected to the EPS directly without PEC as shown

outputs of the permanent magnet generator were connected to a 3ϕ diode rectifier. The output dc voltage across the rectifier was filtered using a capacitor rated at 300 V and 150 μ F. The grid side converter was constructed from a 5 kW, 600 V, 3ϕ , six pulses inverter that was interfaced with a local load rated at a 3ϕ , 208 V, 60 Hz, a 3.3 kW resistive, a 0.5 KVA inductive and a 0.5 KVAR capacitive load. The grid side was obtained from a 3ϕ power supply that was connected to the primary side of a 3ϕ transformer. Details of the system description and inverter control can be found in [9].

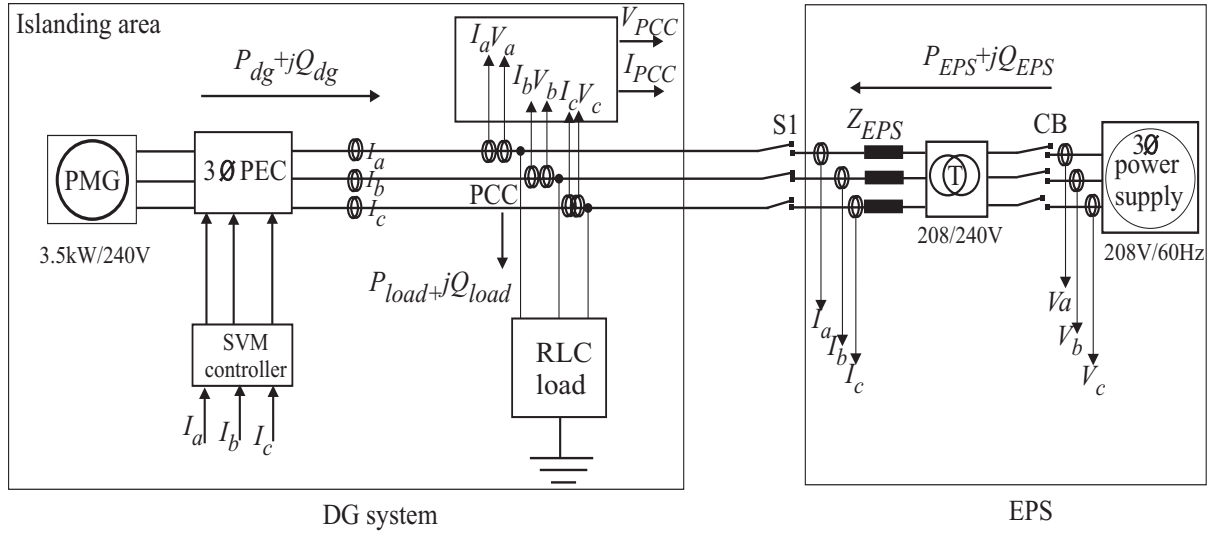


Fig. 5.3: A schematic diagram for the experimental test bed system with PEC.

5.3 Symmetrical Component and WPT

The symmetrical component transform is used to convert three phase voltages and currents into a single phase representation as in [67]. Mathematically, it can be

represented by

$$\begin{bmatrix} V^0 \\ V^+ \\ V^- \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}, \begin{bmatrix} I^0 \\ I^+ \\ I^- \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \quad (5.1)$$

where the V_a, V_b, V_c, I_a, I_b , and I_c designate three-phase line voltages and currents and V^0, V^+, V^-, I^0, I^+ , and I^- , symbolize the zero, positive and negative sequence voltages and currents. The operator a is given as $a = 1\angle 120^\circ$. Only if the three phase system is balanced in such a way that the positive sequence components are non-zero, then the zero and negative sequence components will be zero. From the research, choosing the right data processing techniques is one of the keys for successful anti-islanding algorithms where the islanding artifact is non-periodic, non-stationary, and has a short duration that can be detected. Therefore, the index should be chosen in a way that basically characterizes the topology for reducing the missed alarms that are not based on the signals transform as in [5,65]. The WPT has the features that can be employed to carry out accurate and effective data processing with complex frequency-time structures. Moreover, the WPT accommodates nonuniform bandwidths, such that the bandwidth is higher at higher frequencies, making it possible to implement the wavelet through different levels of decomposition in a filter bank, this symbolizes the advantage of using this method.

The WPT can be mathematically formulated for a discrete signal $y[k]$ as in [55,68,69] and given by equation 5.2:

$$y[k] = \sum_{j \in \mathbb{Z}} \left(\sum_{n \in \mathbb{Z}} a_{j,n}[k] + \sum_{n \in \mathbb{Z}} d_{j,n}[k] \right) \quad (5.2)$$

The approximations $a_j, y[k]$ and details $d_j, y[k]$ are evaluated as

$$a_{(j+1)} = \sum_{n \in \mathbb{Z}} (g[n]a_j[2k-n] + h[n]a_j[2k-n]) \quad (5.3)$$

$$d_{(j+1)} = \sum_{n \in \mathbb{Z}} (g[n]d_j[2k-n] + h[n]d_j[2k-n]) \quad (5.4)$$

where $h[n]$ and $g[n]$ are the respectively half-band low pass (LPF) and high pass (HPF) filters associated with used wavelet basis functions. a_j and d_j are the wavelets approximation and details, respectively. j is the level of decomposition.

5.4 Feature Extraction

Firstly, zero, positive, and negative sequence voltages and currents are extracted from the voltages and currents at the PCC, which are termed symmetrical components $V^0, V^+, V^-, I^0, I^+,$ and I^- and are extracted by Fourier transforms over a sliding window based on the records of the measured three phase voltages and currents at the rated frequency. Equation 5.1 designates the value of each component. Secondly, the zero-sequence impedance of zero-voltages and currents is given by the ratio of the zero sequence voltage to zero sequence current. Then, the ZSI is possessed using the WPT in order to distinguish the islanding. The first level of details and approximations are determined in the same way as in discrete wavelet transform (DWT) [55, 69], where the input signal samples $x_n = [x_0, x_1, x_2, \dots, x_{N-1}]$ with sampling rate f_s , which yields $\Delta t = 1/f_s$. N is the length of the input signal vector. Then, the array of wavelet filter coefficients $(k_1, k_2, k_3, \dots, k_m)$ can be obtained based on the selected mother wavelet, where (n) is an integer number related to the mother wavelet order (n) . In this work, the Debauchees wavelet basis function have a LPF and a HPF with 2^n coefficients for dbn, which is the sliding window is of 2^n length. For example, the

db4 with 8 filter coefficients is used in this investigation, given as

$$\begin{aligned} LPF &= \begin{bmatrix} 00.0106, 00.0329, 00.0308, -00.1870, -0.0280, 00.6309, 0.7148, 0.2304 \end{bmatrix} \\ HPF &= \begin{bmatrix} -0.2304, 0.7148, -0.6309, -0.0280, 0.1870, 0.0308, -0.0329, -0.0106 \end{bmatrix} \end{aligned} \quad (5.5)$$

In order to calculate the approximation, the convolution between the input samples and the LPF coefficients along the sliding window is carried out to provide the first value $[A1]$ of the first approximation array $[a1]$. Then, the window is shifted by two samples to ensure the down-sampling (dyadic scale and binary translation). After that, the second value $[A2]$ of the first approximation array $[a1]$ is calculated in the same manner and so on until the end of the input signal array. Then, the first approximation array $[a1]$ that contains the samples $[A_1, A_2, A_3, \dots, A_M]$ is obtained. M equals the down-sampling, and the sampling rate for the first approximation $[a1]$ is $(f_s/2)$, which yields $\Delta t = 1/(f_s/2) = 2\Delta t$. The first stage of the WPT analysis ($j = 1$), $a1; n[x]$ and $d1; n[x]$ are evaluated as in [69]. For example, in the first detail $[d1]$, the same procedure was repeated using the HPF instead of LPF coefficients. Here, the second level arrays $[a1]$ and $[d2]$ are obtained using the same process as for level 1, using array $[a1]$ with length M as the input signal. The detection algorithm drills down to the second level of decomposition and implements the filtering operation as follows:

$$a1[x] = \sum_{i=0}^{N-1} h[g]x[n-i] \quad (5.6)$$

$$aa1[x] = \sum_{i=0}^{N-1} h[g]a1[n-i] \quad (5.7)$$

$$d1[x] = \sum_{i=0}^{N-1} h[k]x[n-i] \quad (5.8)$$

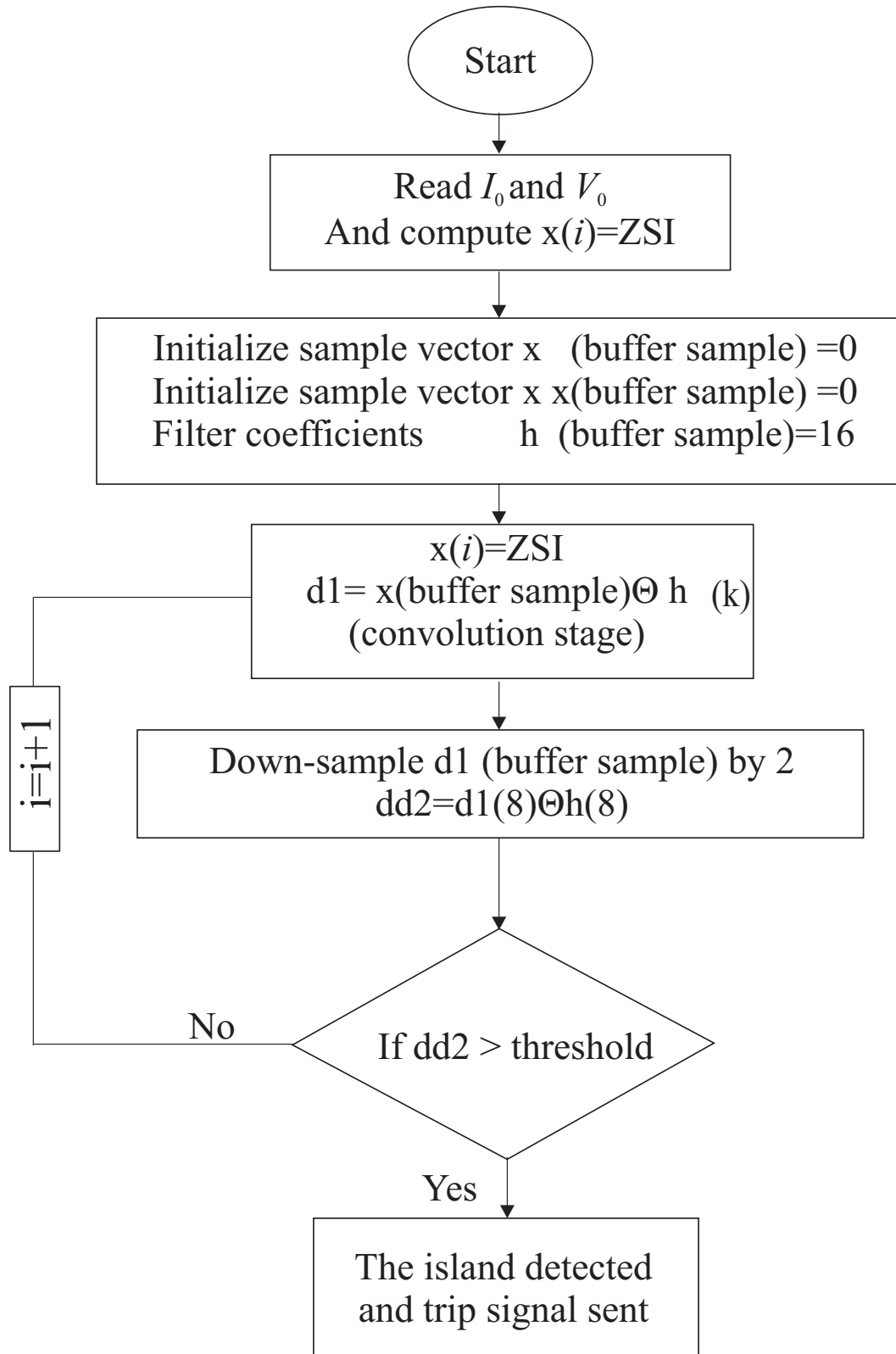


Fig. 5.4: The Flowchart of Wavelet based detection.

$$dd2[x] = \sum_{i=0}^{N/2-1} h[k]d1[n-i] \quad (5.9)$$

where $h[g]$ of length N are the coefficients of the LPF, and $h[k]$ of length N are the coefficients of the HPF, and $d1[n-i]$ denotes the array details (high-frequency band) resulting from the decomposition of the discrete signal ($x[n]$), which represents the discrete signal of ZSI.

5.5 Anti-islanding Algorithm

A MATLAB code is implemented using a sliding window of 16 samples with a sampling frequency of 30 kHz, as shown in the flow chart in 5.4. The detection algorithm considers the input signal $x[n]$ as a vector of successive samples of the ZSI and is denoted by $x[n] = [x_0, x_1, x_2, \dots, x_N]$, where x_0, x_2 , and x_3 are the samples of the input signal $x[n]$, and N is the length of input signal. The WPT filter coefficients are denoted as $h[k]$ of length m , where k is the HPF coefficients and m is the length of the selected db4 wavelet filter coefficients, as noted above.

At the first stage of the algorithm, variables, V^0 and I^0 , are initialized to zero, then the detailed array (high frequency content of the input signal) is calculated by the circular convolution of the input samples x [69] with the HPF coefficients along the sliding window to get the first array approximation value $a1$ and detailed value $d1$. $d1$ denotes the array of high-frequency content in the first level of decomposition at $j = 1$, and j denotes the level of decomposition as represented in equations (5.3) and (5.4). Furthermore, in the same manner, the WPT allows using LPF coefficients to calculate the array of approximation at each level (low-frequency content of the input signal) using equation (5.4).

At the second level, the down-sampling factor is 2. The convolution is done between the input signal ($d1$) and the HPF along the sliding window to obtain the second

array detailed value (dd2), which is represented mathematically in equation (5.9). Islanding is detected and a trip signal is activated under the conditions as described by

$$ZSI = \left| \sum_{k=0}^{N-1} dd2 \right| > threshold \quad (5.10)$$

The ZSI based on WPT is computed as follows, and the WPT computes the change of the zero sequence voltage and current that are denoted by

$$v_x(t) = v_{j,x}^0 + \sum_{n=1}^{2j-1} v_{j,x}^{0,n} \quad (5.11)$$

$$i_x(t) = i_{j,x}^0 + \sum_{n=1}^{2j-1} i_{j,x}^{0,n} \quad (5.12)$$

where x denotes the zero-sequence voltage ($v_{j,x}^0$) and zero-sequence current ($i_{j,x}^0$) at any phase A , B , and C at node 0. The $v_{j,x}^{0,n}$ and $i_{j,x}^{0,n}$ are zero-sequence voltage and current, respectively, at any $n \neq 0$, and j denotes the wavelet decomposition level. The ZSI is defined by

$$ZSI = \sum_{n=1}^{2j-1} [v_{j,x}^{0,n} / i_{j,x}^0] \quad (5.13)$$

$$ZSI = \sum_{n=1}^{2j-1} [v_{j,x}^{0,n} / i_{j,x}^0] \quad (5.14)$$

5.6 Evaluation Criteria

The performance of the proposed index, in both inverter systems and non inverter systems, is assessed, and numerous conditions are investigated for both selecting the mother wavelet and the number of resolution levels. The following scenarios represent the worst case scenario that this research focuses on.

- i) Load matches the DG output when islanding occurs;
- ii) Load change from 0% to 20 %;

- iii) Unbalanced load caused by changes in the phase resistance, capacitance, and inductance; and
- iv) Power Quality disturbances including voltage sag, voltage swell, and harmonics.

5.7 Simulation Tests and Discussion

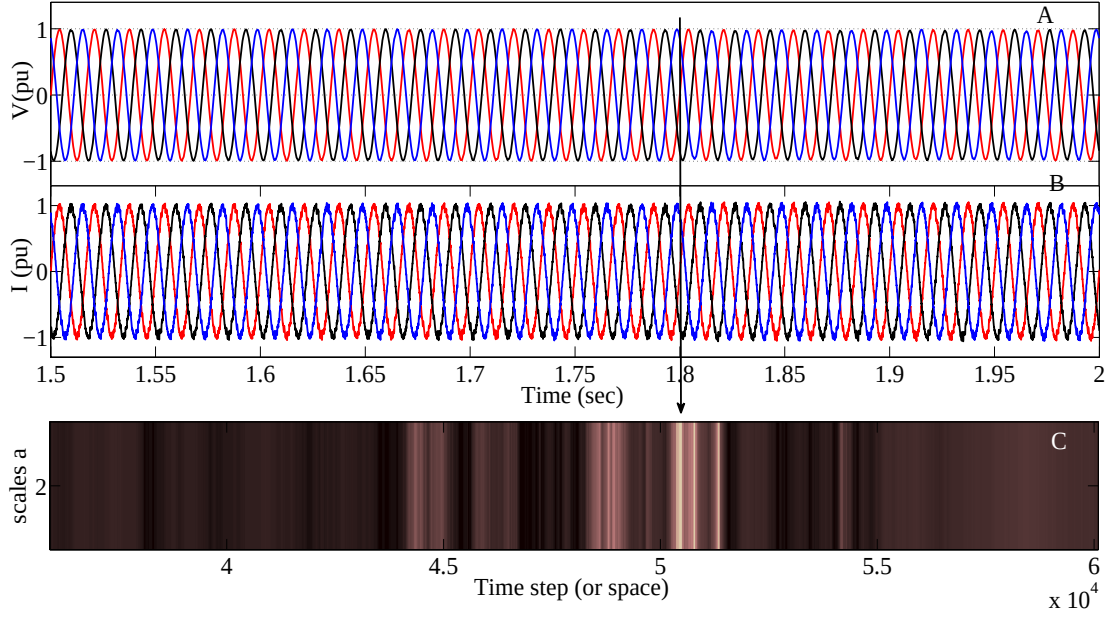


Fig. 5.5: Voltage and current at PCC next to the wavelet coefficients for ZIS at the condition of load matches DG output in inverter-based system.

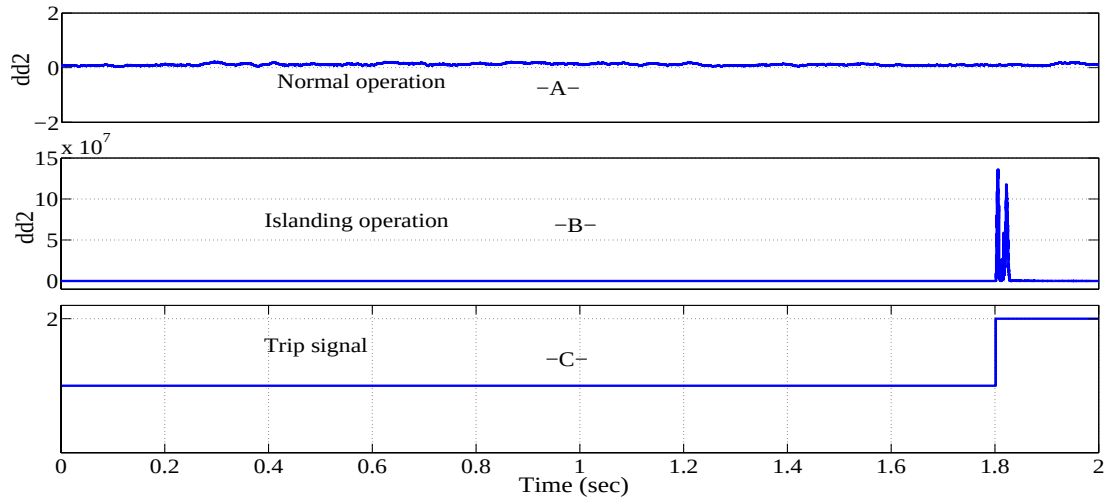


Fig. 5.6: Algorithm response for both normal and islanding operation and their trip signal in inverter-based system.

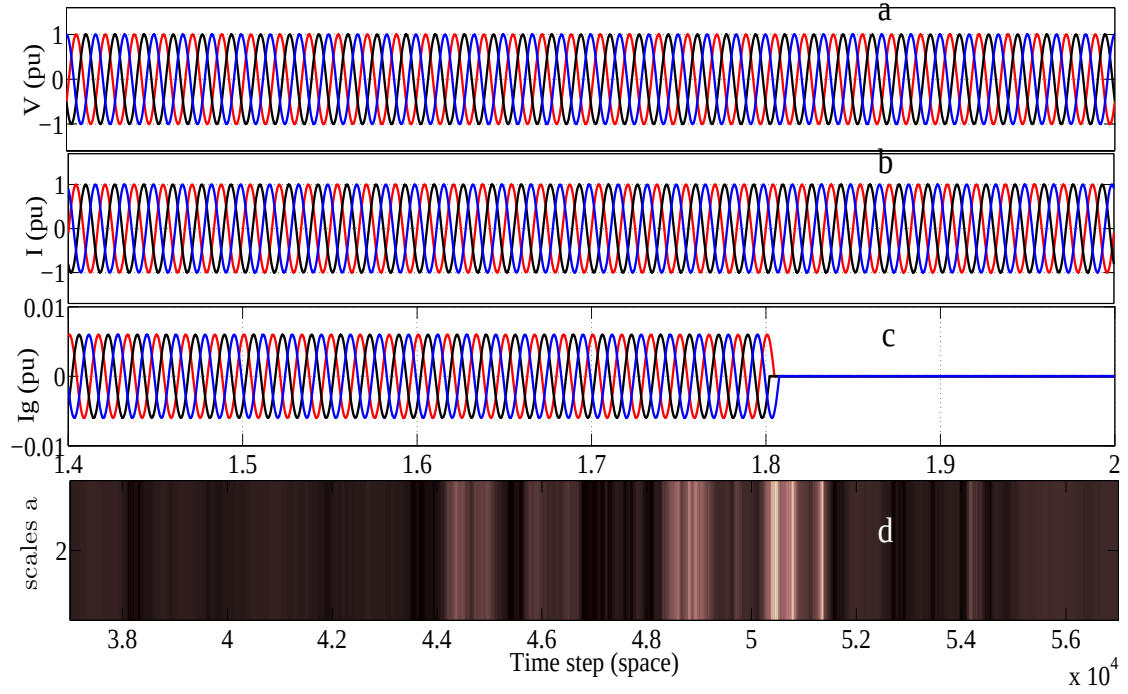


Fig. 5.7: (a) Voltages at the PCC, (b) the currents at PCC, (c) the currents at EPS side, (d) the wavelet coefficients for ZIS at the condition of load, which matches the DG output in non-inverter-based system.

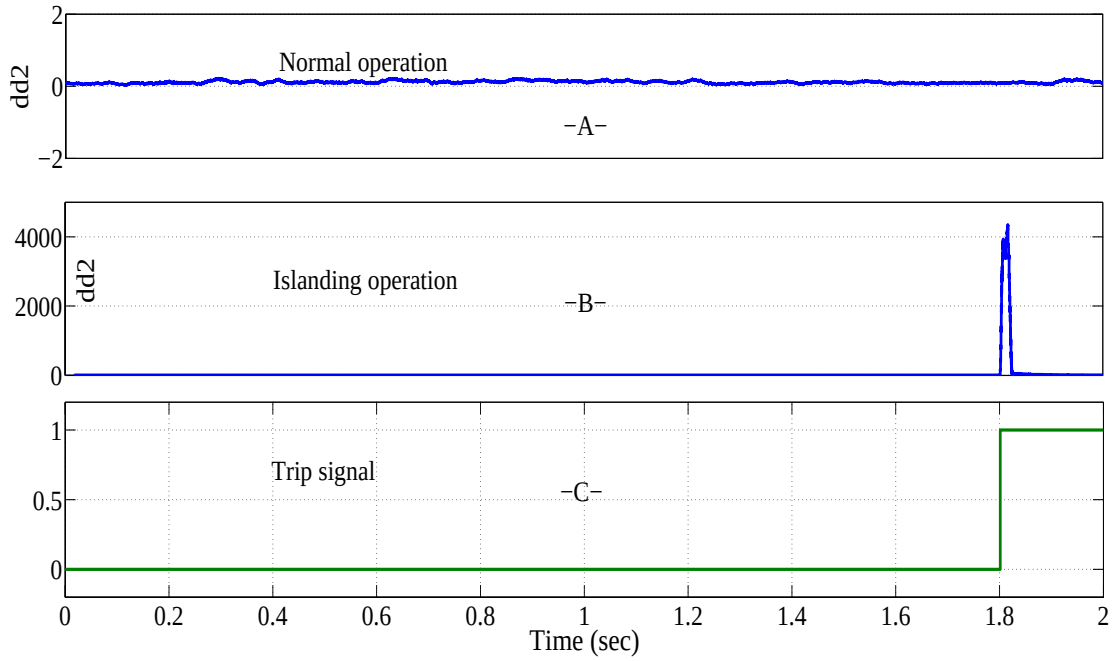


Fig. 5.8: Algorithm response for both normal and islanding operation and their trip signal in non-inverter-based system.

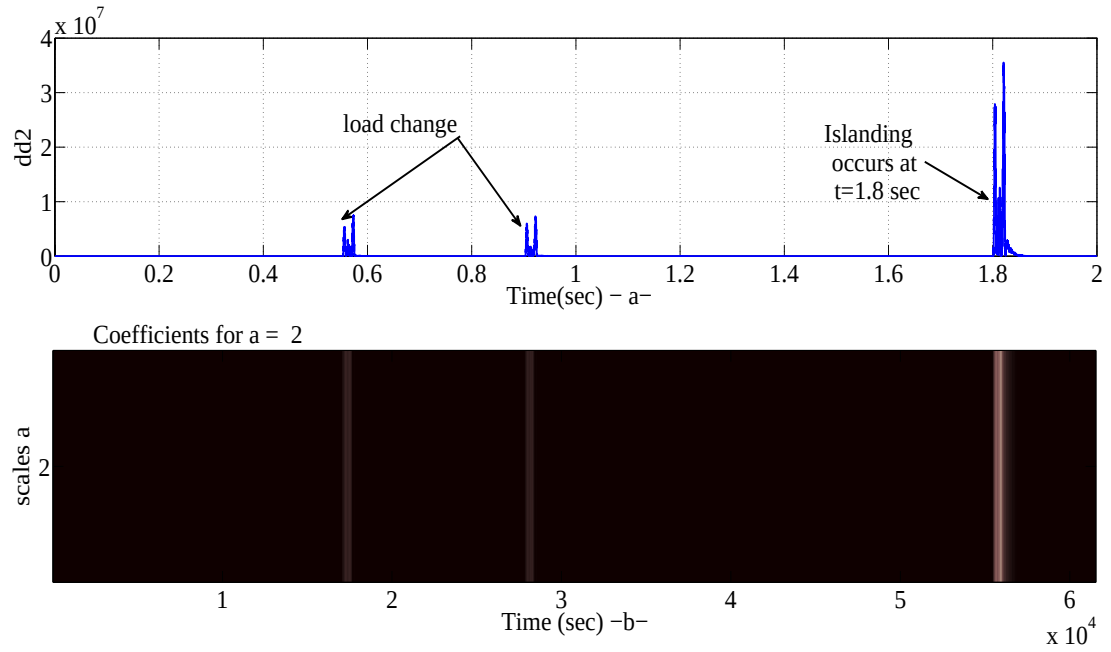


Fig. 5.9: Wavelet distinguish response on the condition of unbalanced load and island subjected to inverter-based system.

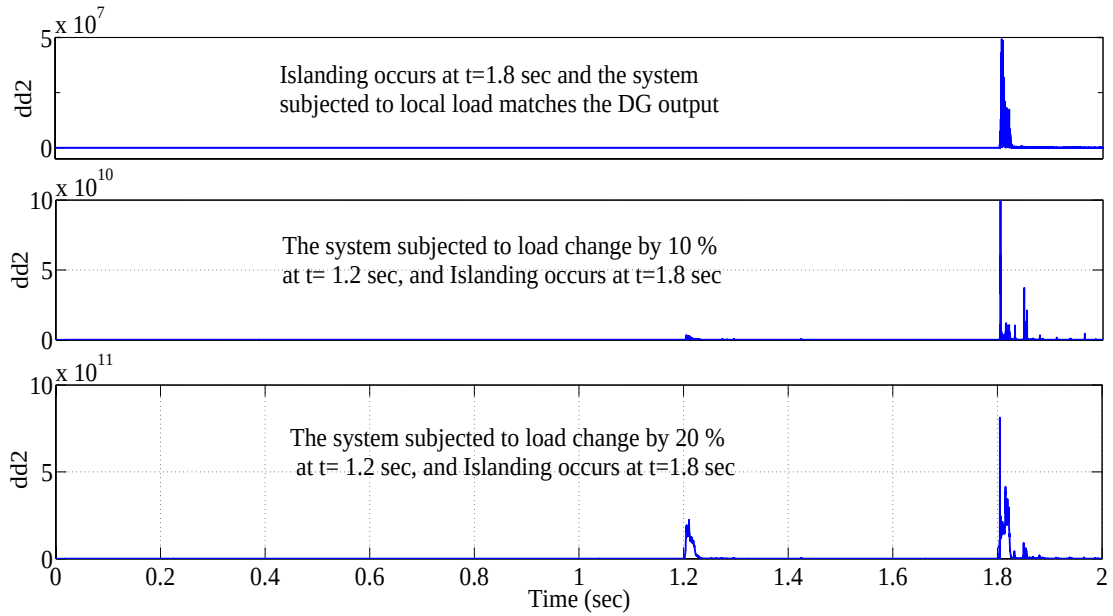


Fig. 5.10: Algorithm response on the ZIS for both normal and islanding operation and their trip signal in inverter-based system.

Fig. 5.5(A) and Fig. 5.5(B) show the measured 3ϕ voltage and current when the island suddenly occurs in systems with PEC. Fig. 5.5(C) show the existence of wavelet details' coefficients and their time location for islanding operation at the second level dd2. The results show that the bands indicating the values of evaluated coefficients are brighter, thus making them distinguishable and providing an accurate diagnosis in islanding operation. As an example, load changes seen in Fig. 5.9 that are based on variations in signal energy. Fig. 5.6(A) and Fig. 5.6(B) show the detailed decomposition of the ZSI at the second level as the system transitions from a non-islanding state into an islanding state. The trip signal, as shown in Fig. 5.6(C), is triggered when the second level high frequency sub-band component exceeds a predefined threshold. Fig. 5.7(a) and Fig. 5.7(b) show the measured 3ϕ voltage and current when the island suddenly occurs in systems without PECs. Fig. 5.7(d) shows the existence of wavelet details' coefficients and their time location for islanding operation at the second level dd2. Fig. 5.7(c) shows the EPS current flowing to the DG side, which is almost equal to zero. Fig. 5.8(A) and Fig. 5.8(B) show the detailed decomposition of the ZSI at the second level as the system transitions from a non-islanding state into an islanding state. The trip signal, as shown in Fig. 5.8(C), is triggered when the second level high frequency sub-band component exceeds a predefined threshold. Also, the investigation includes the effect of a load change in inverter-based systems and the results are illustrated in Fig. 5.9(a). From the results, it is very possible and distinguishable in Fig. 5.9 (b) that during islanding amplitude and variations of energy in the signal are changed. The results provide certain features for each case studied, hence making them distinguishable. Fig. 5.10 shows the detailed decomposition of the ZSI at the second level as the system is subjected to a load change of 10 % - 20 %. These features can be thought of as signatures, which are able to provide an accurate diagnosis of different cases. The desired signature is the values and the time locations of the coefficients of the second

level details dd2 . The WPT based islanding detection can be realized by evaluating the coefficient of the wavelet details and comparing their values in the second level highest frequency sub-band to zero.

5.8 Experimental Tests and Discussion

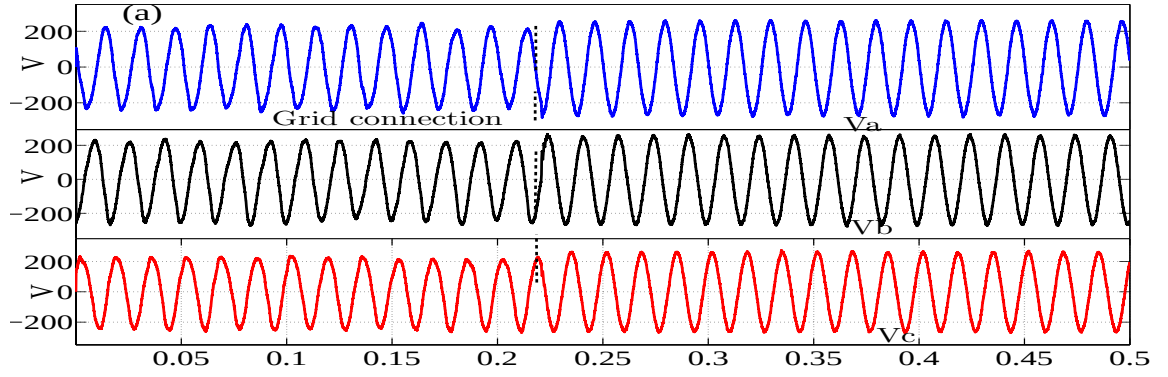


Fig. 5.11: Phases voltage at the PCC.

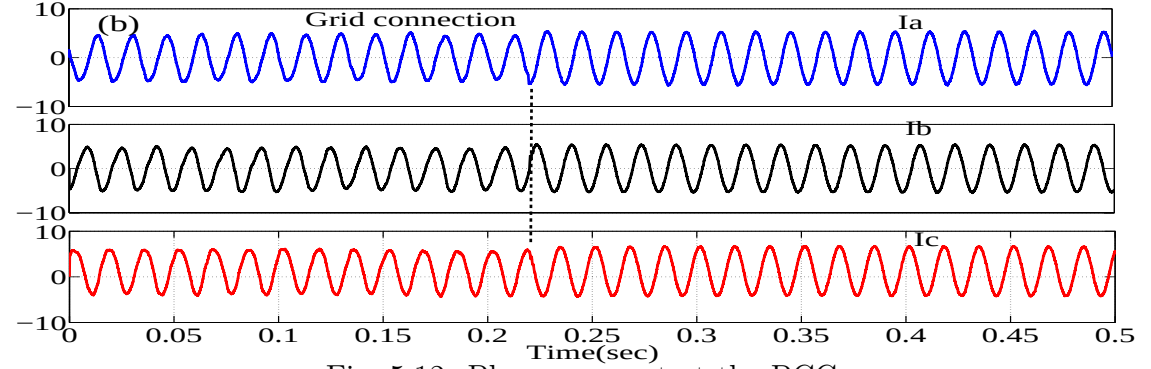


Fig. 5.12: Phases current at the PCC.

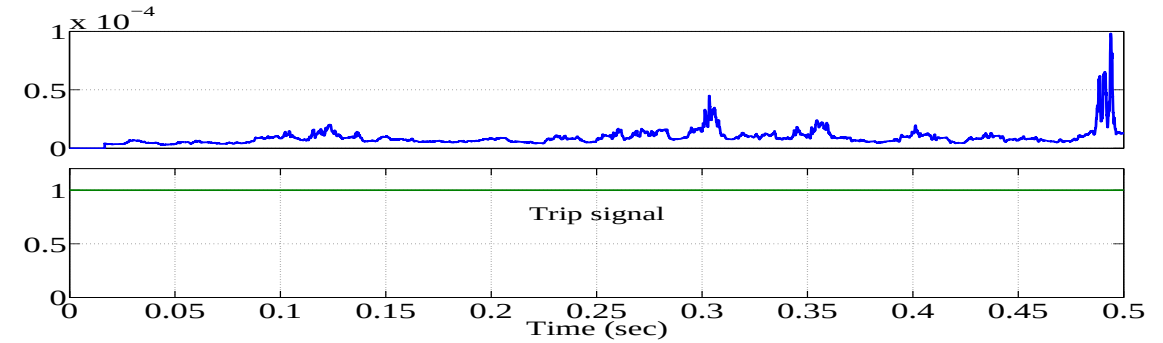


Fig. 5.13: The ZIS magnitude and the algorithm response and their trip signal.

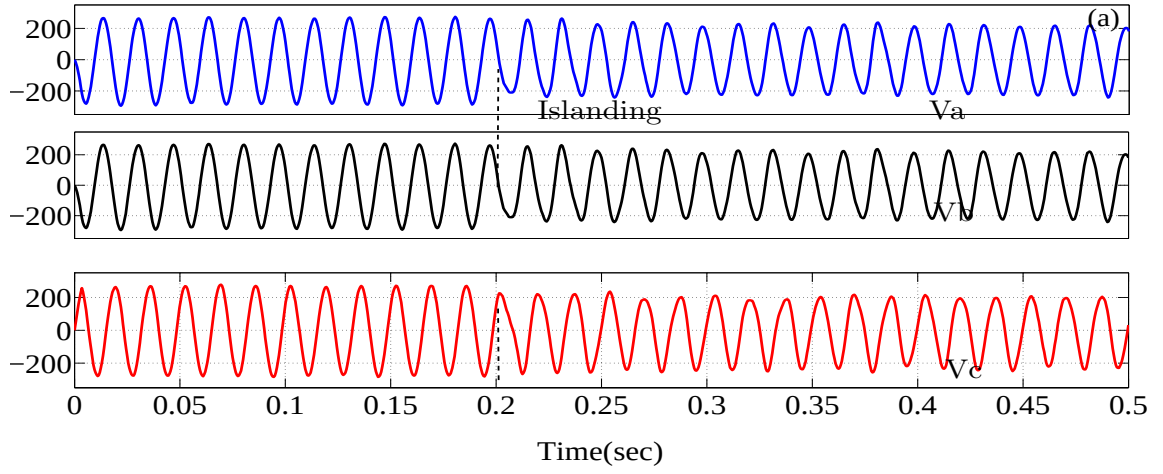


Fig. 5.14: Phases voltage at the PCC.

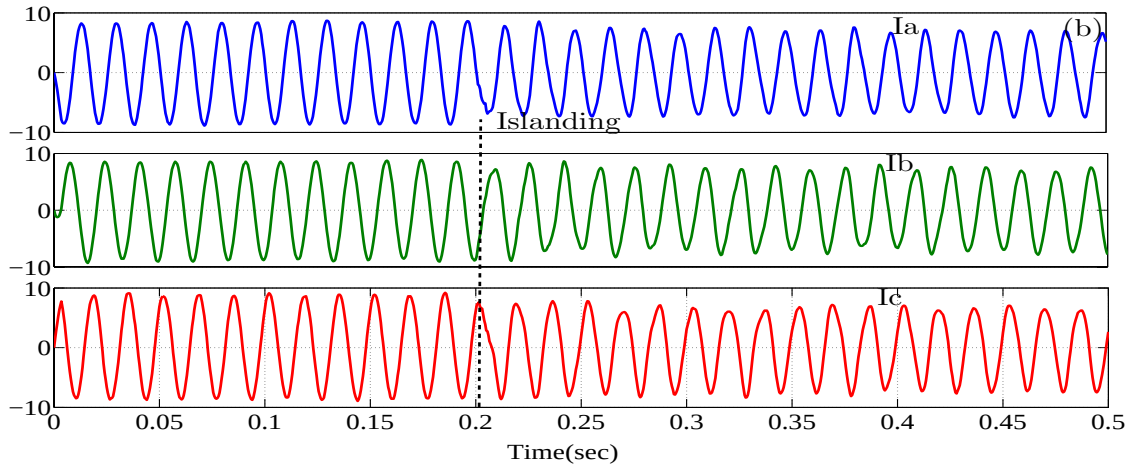


Fig. 5.15: Phases current at the PCC.

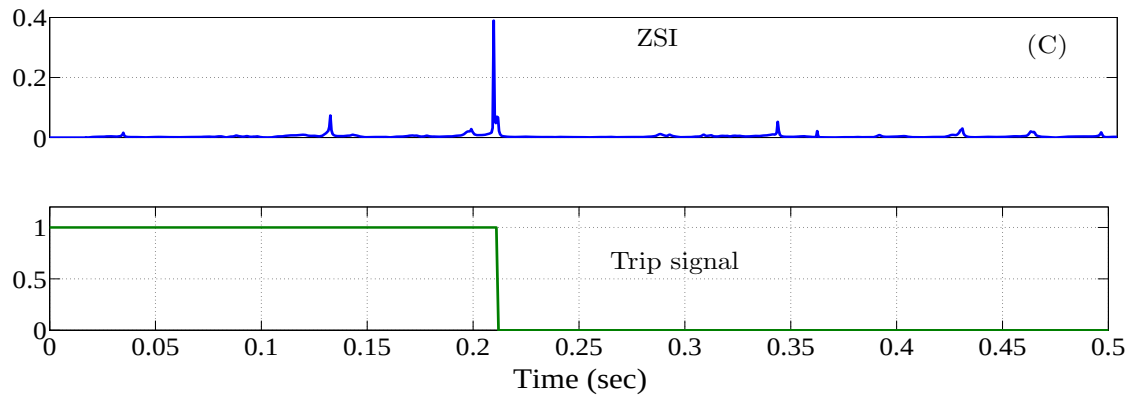


Fig. 5.16: ZIS magnitude and the algorithm response on islanding operation and their trip signal.

The results are generated from lab tests and the most two interesting scenarios during lab tests were testing the algorithm against the grid connection event and how the algorithm was able to identify the islanding operation in the case of balanced power between DG and EPS. The phases of voltage V_a , V_b , and V_c at PCC can be seen in Fig. 5.11, while current phases I_a , I_b , and I_c , can be seen in Fig. 5.12.

Fig. 5.11 and Fig. 5.12 represented the grid connection scenario along with the normal operation, and the moment of DG integrated to EPS at time of $t = 0.202$ sec, followed by the trip signal that was computed based on equation (5.9). This remained unchanged during this operation scenario due to the almost zero value of ZSI as shown in Fig. 5.13. However, during the islanding scenario, the voltage and current are shown in Fig. 5.14. and Fig. 5.15, where the algorithm identified the islanding event at $t = 0.205$ sec. The trip signal is changed to stat of zero at 0.211 msec after the islanding operation took place. This time is very short compared with the standard response time of 2 sec. Furthermore, the algorithm accuracy is tested at balanced power scenarios.

5.9 Summary

The chapter presents the development and performance evaluation of a new passive anti-islanding index extracted using the WPT. The WPT provides an accurate decomposition for non-stationary signals, such as the ZSI. The introduced method has advantages over existing schemes in terms of the simplicity with it which can be implemented into DSP and the accuracy of its response. The results show accurate identification of the islanding event. Furthermore, it may be a universal for a three-phase system in the sense that it is applicable for both inverter and non-inverter based distributed generators. The algorithm is verified using the simulation of inverter based and non-inverter based DG systems with various types of disturbances.

The algorithm is also tested using the off-line data records of islanding events. The results show that the detection is improved in terms of missed alarm rates under load change up to 20 % in both DG systems that have EPC and DG systems that do not have EPC. Furthermore, the results show the validity of the index in different interconnection topologies in comparison with [9,65]. The research contribution presented in this chapter includes a new index for passive methods, which found a common ground between DG systems with the EPCs and DG systems without the EPCs that may be used as a feature for three-phase systems.

Chapter 6

Conclusions

The summary and contributions of this research, along with recommendations for future work, are highlighted in this chapter.

6.1 Summary

A detailed investigation on the state-of-the-art passive anti-islanding developments has been achieved, by reviewing related publications over the past two decades. It has been found that the main concern of these methods is the high level of detection errors that are characterized by false and missed alarms. Furthermore, passive islanding detection methods have no impact on the EPS and are easy to implement. However, they possess a shortcoming characterized by NDZ resulting in unsafe operation.

This dissertation has presented a new passive anti-islanding methodology for the utility interconnection of distributed generation that improves islanding detection in terms of missed alarms compared to conventional anti-islanding schemes along with introducing new indices to the passive methods.

The demonstrated methodology is based on the frequency dependent impedance (FDI) concept. The methodology characterizes the change of interconnection topology and employed this change as a basis for islanding detection. The use of a frequency

spectrum decomposition of measured voltage and current that exploits the presence of harmonic distortion at the PCC, as seen by DG, has been the basis of the impedance computation metric. The following is a summary of the methodology.

Firstly, the characterization of the change of the interconnection topology is analytically done using an electric circuit model, which was used to derive a transfer function of the impedance at the PCC. The impedance is chosen because it reflects the interconnection topology. The transfer function characterizes the physical impedance as seen by DG, which in turn characterizes the impedance during normal and islanding operations. The feature that distinguishes islanding operation is extracted from frequency response characterization; then, the frequency response characterization is used as the basis of detection logic. However, in practical terms, the impedance may be calculated using the FFT of the measurements of the voltage and current at the PCC at those frequencies where there is sufficient harmonic content. As an example the odd harmonics, 3^{th} , 5^{th} , 7^{th} , 9^{th} , 11^{th} , 13^{th} , and 15^{th} may be selected when the impedance computed. Moreover, the FDI is verified analytically, in simulation and experimentally. The results show reliable and accurate improvement of islanding detection in terms of missed alarms compared with the existing schemes.

This research is distinguished over the previous research by i) the use of an index that reflects the interconnection topology rather than employing signal heuristics that in most cases demonstrate a high level of detection errors; ii) the focus on a range of frequencies that provide more information at the feature extraction stage, which allows the detection logic to make a reliable decision instead of single frequency, which in some operating conditions does not provide enough information to detection-logic resulting in an unreliable decision; and iii) being able to extend to different distributed generators and to multiple generators with various operating and load conditions and for different interconnection topologies due to the decision making being independent of excitation.

In addition, the dissertation presents a new passive anti-islanding approach based on VPS, which is implemented in the independent hardware using TMS320F28335, a Digital Signal Processor (DSP) in the inverter based system. This islanding detection hardware offers a wide range of different interconnection topologies, either with the interconnection using the EPCs or without using the EPCs. The index is obtained from a product of spectral decompositions of voltage and current at the PCC. The approach introduced provides accurate detection in a timely manner.

Finally, the dissertation presents the ZSI as a new index for islanding detection based on WPT as the time frequency dependent index. The method provides secure islanding detection at load resonant frequency and percentage of load variation.

6.1.1 Overview of Contributions

The major contributions of this dissertation to the field of anti-islanding are as follows:

- New methodology using the measurement of voltage and current at the PCC for islanding detection based on the FDI concept is introduced [70]. The advantage of FDI is it is based on the change of system topology, unlike signal heuristics that are based on transient signals [9, 15].
- Establishing an index for islanding detection with improved anti-islanding performance in the operation space where existing schemes fail [40]. The index is based on voltage and current at different frequencies that improve the islanding detection with respect to missed alarms, unlike [11], which focused on simulation based on multi-indices of power flow at single frequency.
- Confirmation is achieved of the equivalence of using the electrical circuit model and using the measurements of time-series data of voltage and current to compute the index of anti-islanding protection. The linking of the parametric model

and non-parametric model that is based on the measurements of time-series data of voltage and current is introduced; it may be possible to use the non parametric model as a basis of islanding detection and threshold selection in a different interconnection topology with varied operating conditions that are not included in this dissertation.

- Independent hardware is designed and tested online [64], which is specified for islanding detection. However, whereas most existing anti-islanding schemes are embedded within PECs as in [56], this hardware is designed independent of PECs, which allows for use in different interconnection topologies.
- The VPS approach is introduced as a passive islanding detection scheme that has been tested online and validated in simulation where its decision-making mechanism provides accurate, reliable, and timely islanding detection [64].
- The ZSI index is introduced [71] as an anti-islanding detection scheme that provides highly sensitive islanding detection of up to 20% load variation. The introduced index has advantages over existing schemes [15, 66] in terms of simplicity, accuracy of response, and latency. Furthermore, the results show the ZSI index may be applicable as an index for both inverter and non-inverter based distributed generations.

6.2 Recommendations for Future Work

The following extensions to the work presented here would be very interesting:

- Extending proposed approaches to systems with multiple distributed generators for different interconnection topologies.
- Implementing FDI into DSP and conducting online testing with multi-DGs would be an extremely challenging scenario but could be possible.

6.3 Final Comments

A reliable, accurate, and timely anti-islanding technology is key to the large-scale deployment of renewable-energy sources. Reliable islanding detection that meets the interconnection standards permits a widespread penetration of renewable technology into the electricity market that improves the environment and reduces the cost of electricity.

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Appendix A

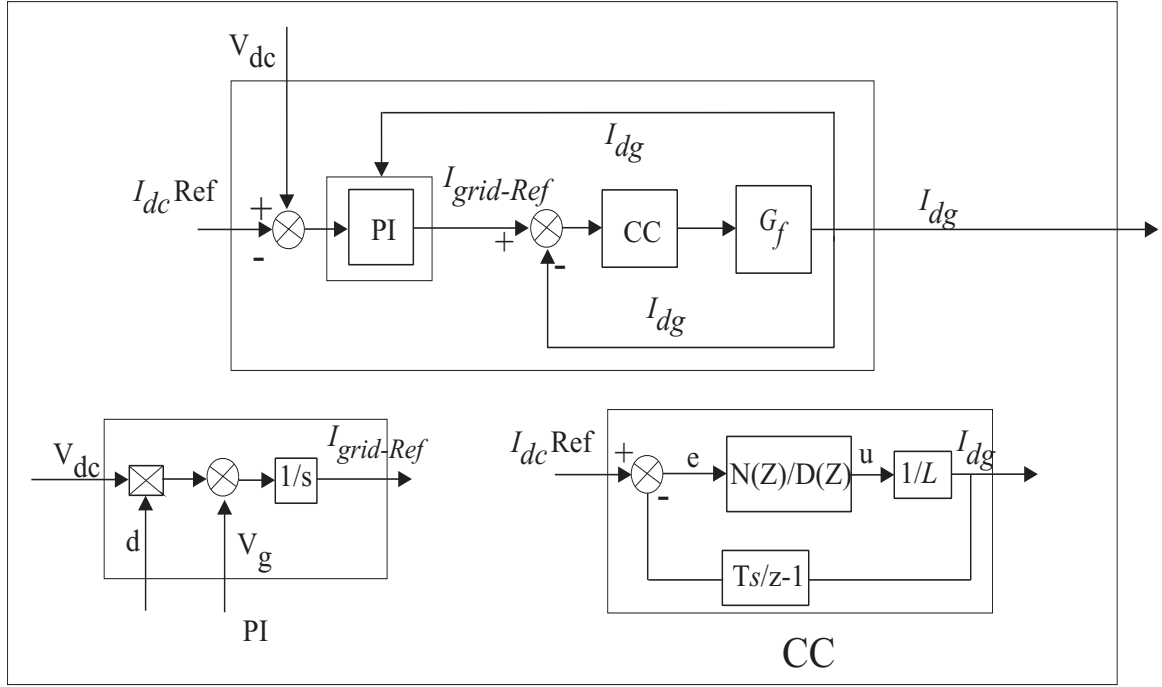
Appendixes

A.1 Inverter Control Scheme

Fig. A.1. shows the inverter control of the inverter Model 112-60 that described in model details in [59]. The inverter Model 112-60 was used for experimental test bed, where consist of PI controller for voltage compensator. The reference voltage of the controller for the inverter is set to a value that determined by the amplitude of the grid voltage. The I_{dg} is the controlled variable, which is usually controlled to track a sinusoidal current reference; d is the manipulated variable, which calculated by the DSP; V_{dc} and V_g are voltage of DC link and grid voltage and are used regarded as disturbances to the plant. CC is the predictive current controller that is based on the discrete Transfer function as described in details in [59, 60], to ensure the best dynamic response with todays DSP technology. More details can be found in [59]. Fig. A.2 shows the a photo of the inverter model I12-60. The specifications of the inverter appears in Table. A.1.

Table A.1: Inverter Model I12-60 Specified Parameters

Rated maximum continuous AC output power	12 kW
Maximum continuous AC output current	50 A
Power Factor	1
Current THD at rated output current	$\leq 2\%$
Nominal single phase grid voltage	240 V
Nominal Grid frequency	60 Hz



Inverter controller

Fig. A.1: Control diagram of the inverter Model 112-60.



Fig. A.2: A photo of the physical inverter

A.2 Mathematical Exploration for System Identification

In order to identify a system using time series measurements, this section mathematically shown the steps. A system can be represented by following transfer function,

$$G(s) = \frac{n(s)}{d(s)} = \frac{s^m + b_{m-1}s^{m-1} + \dots + b_1s + b_0}{s^n + a_{n-1}s^{n-1} + \dots + a_1s + a_0} \quad (\text{A.1})$$

where $n \geq m$, and all the a and b coefficients are real numbers. n and m represent the order of numerator and the denominator of the transfer function. Also,

$$H = \frac{n(s)}{d(s)} = \frac{n(j\omega)}{d(j\omega)} \quad (\text{A.2})$$

It can be expand as function of s,

$$\frac{n(s)}{d(s)} = \frac{a_0 + a_1(s) + a_2(s)^2 +j^N a_N s^N}{1 + b_1(s) + b_2(s)^2 +j^N b_N s^N} = B_{Re}(j\omega) + jB_{Im}(j\omega) \quad (A.3)$$

It can be expressed as function of ω

$$\frac{n(s)}{d(s)} = \frac{a_0 + a_1 j\omega + a_2 j\omega^2 +j^N a_N \omega^N}{1 + b_1 j\omega + b_2 j\omega^2 +j^N b_N \omega^N} = B_{Re}(j\omega) + jB_{Im}(j\omega) \quad (A.4)$$

From the time series measurements of voltage, U, and current, Y, the FFT of U and Y can computed as

$$\text{FFT}(U) \rightarrow [\text{Re}(U); \text{Im}(U)] \quad (A.5)$$

$$\text{FFT}(Y) \rightarrow [\text{Re}(Y); \text{Im}(Y)] \quad (A.6)$$

The transfer function, H, that represents in this case the impedance can be computed using equation (A.7) where time series measurements of U and Y are used. The impedance represents so called black box of the system model.

$$H = \frac{Y(s)}{U(s)} = \frac{[Re(Y) + jIm(Y)]}{[Re(U) + jIm(U)]} \quad (A.7)$$

$$H = \frac{[Re(Y) + jIm(Y)] [Re(U) - jIm(U)]}{[Re(U) + jIm(U)] [Re(U) - jIm(U)]} \quad (A.8)$$

$$H = \frac{[Re(Y) \times Re(U) + Im(Y) \times Im(U)] + j [Im(Y) \times Re(U) - Re(Y) \times Im(U)]}{[(Re(U))^2 + (Im(U))^2]} \quad (A.9)$$

$$H = Re(H) + jIm(H) \quad (A.10)$$

$$\frac{a_0 + a_1(s) + a_2(s)^2 + ...j^N a_N s^N}{1 + b_1(s) + b_2(s)^2 + ...j^N b_N s^N} = [Re(H) + jIm(H)] = [Re + jIm] \quad (A.11)$$

To find transfer function coefficient as example of the second order system

$$\frac{a_0 + a_1s + a_2s^2}{b_0 + b_1s + s^2} = [Re(H) + jIm(H)] = [Re + jIm] \quad (A.12)$$

To find transfer function coefficients, the ordinary Least Squares (OLS) solutions is used in order to estimate unknown parameters as explored in the following:

$$AX = B \quad (A.13)$$

Where, A= (3.25); ; B=(3.26) The full matrix for a range of frequencies can be expressed as following

$$\begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ \vdots \\ A_n \end{bmatrix} \times \begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ b_0 \\ b_1 \end{bmatrix} = \begin{bmatrix} B_1 \\ B_2 \\ \vdots \\ \vdots \\ B_n \end{bmatrix} \quad (A.14)$$

where :

$$\begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ b_0 \\ b_1 \end{bmatrix} = \text{pinv} \begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ \vdots \\ A_n \end{bmatrix} \times \begin{bmatrix} B_1 \\ B_2 \\ \vdots \\ \vdots \\ B_n \end{bmatrix}$$

For example of second order system,

$$\frac{a_2s^2 + a_1s + a_0}{s^2 + b_1s + b_0} = Re + jIm \quad (A.15)$$

$$\frac{-a_2\omega^2 + ja_1\omega + a_0}{-\omega^2 + jb_1\omega + b_0} = Re + jIm \quad (A.16)$$

$$[(a_0 - a_2\omega^2) + ja_1\omega = (R + jI) ((b_0 - \omega^2) + jb_1\omega)] \quad (A.17)$$

$$\begin{aligned}
(a_0 - a_2\omega^2) + ja_1\omega &= (R + jI)((b_0 - \omega^2) + jb_1\omega) \\
&= R(b_0 - \omega^2) + jRb_1\omega + jI(b_0 - \omega^2) - Ib_1\omega
\end{aligned} \tag{A.18}$$

$$(a_0 - a_2\omega^2) + ja_1\omega - R(b_0 - \omega^2) - jRb_1\omega - jI(b_0 - \omega^2) + Ib_1\omega = 0$$

$$(a_0 - a_2\omega^2) - Rb_0 + Ib_1\omega = -R\omega^2$$

$$a_1\omega - Rb_1\omega - Ib_0 = -I\omega^2$$

$$\begin{bmatrix} 1 & 0 & -\omega^2 & -R & I\omega \\ 0 & \omega & 0 & -I & -R\omega \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ b_0 \\ b_1 \end{bmatrix} = \begin{bmatrix} -R\omega^2 \\ -I\omega^2 \end{bmatrix} \tag{A.19}$$

For the third order system

$$\frac{a_3s^3 + a_2s^2 + a_1s + a_0}{s^2 + b_2s^2 + b_1s + b_0} = Re + jIm \tag{A.20}$$

$$\frac{-ja_3\omega^3 - a_2\omega^2 + ja_1\omega + a_0}{-j\omega^3 - b_2\omega^2 + jb_1\omega + b_0} = Re + jIm \tag{A.21}$$

$$(a_3\omega^3 - a_1\omega) - a_2\omega^2 + a_0 = R(-j\omega^3 - b_2\omega^2 + jb_1\omega + b_0) + jI(-j\omega^3 - b_2\omega^2 + jb_1\omega + b_0) \tag{A.22}$$

$$(a_3\omega^3 - a_1\omega) - a_2\omega^2 + a_0 = R(-j\omega^3 - b_2\omega^2 + jb_1\omega + b_0) + jI(-j\omega^3 - b_2\omega^2 + jb_1\omega + b_0)$$

$$-(a_3\omega^3 - a_1\omega) = R(-\omega^3 + b_1\omega) + I(-b_2\omega^2 + b_0)$$

$$-a_2\omega^2 + a_0 = R(-b_2\omega^2 + b_0) + I(\omega^3 - b_1\omega) \tag{A.23}$$

$$\begin{aligned}
& -(a_3\omega^3 - a_1\omega) - R(b_1\omega) - I(-b_2\omega^2 + b_0) = -R\omega^3 \\
& -a_2\omega^2 + a_0 - R(-b_2\omega^2 + b_0) - I(-b_1\omega) = I\omega^3
\end{aligned}$$

$$\begin{bmatrix} 1 & 0 & -\omega^2 & -R & I\omega \\ 0 & \omega & 0 & -I & -R\omega \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ b_0 \\ b_1 \end{bmatrix} = \begin{bmatrix} -R\omega^2 \\ -I\omega^2 \end{bmatrix} \quad (\text{A.24})$$

$$\begin{bmatrix} 0 & \omega & 0 & -\omega^3 & -I & -R\omega & I\omega^2 \\ 1 & 0 & -\omega^2 & 0 & -R & I\omega & R\omega^2 \end{bmatrix} = \begin{bmatrix} -R\omega^3 \\ I\omega^3 \end{bmatrix}$$

As summary in the order of the system (s),

$s = 2$

$$\begin{bmatrix} 1 & 0 & -\omega^2 & -R & I\omega \\ 0 & \omega & 0 & -I & -R\omega \end{bmatrix} X = \begin{bmatrix} -R\omega^2 \\ -I\omega^2 \end{bmatrix}$$

$s = 3$

$$\begin{bmatrix} 0 & \omega & 0 & -\omega^3 & -I & -R\omega & I\omega^2 \\ 1 & 0 & -\omega^2 & 0 & -R & I\omega & R\omega^2 \end{bmatrix} X = \begin{bmatrix} -R\omega^3 \\ I\omega^3 \end{bmatrix}$$

$s = 4$

$$\begin{bmatrix} 1 & 0 & -\omega^2 & 0 & \omega^4 & -R & I\omega & R\omega^2 & -I\omega^3 \\ 0 & \omega & 0 & -\omega^3 & 0 & -I & -R\omega & I\omega^2 & R\omega^3 \end{bmatrix} X = \begin{bmatrix} R\omega^4 \\ I\omega^4 \end{bmatrix}$$

$s = 5$

$$\begin{bmatrix} 1 & 0 & -\omega^2 & 0 & \omega^4 & 0 & -R & I\omega & R\omega^2 & -I\omega^3 & -R\omega^4 \\ 0 & \omega & 0 & -\omega^3 & 0 & \omega^5 & -I & -R\omega & I\omega^2 & R\omega^3 & -I\omega^4 \end{bmatrix} X = \begin{bmatrix} -I\omega^5 \\ R\omega^5 \end{bmatrix} \quad (\text{A.25})$$

Table A.2: Simulation System Parameters for PEC Based System and no PEC Based System

Grid side parameters	240 V/ 60 Hz
Transformer	12 KVA
Power Factor	1
load	240/ 10 kW
DG side	240/ 60 Hz - 10 kW
A synchronous machine	squirrel cage Hz 15 kW

Vita

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1. S. A. Saleh, A. S. Aljankawey, R. Errouissi, and E. Castillo-Guerra, "Extracting the Phase of Fault Currents: A New Approach for Identifying Arc Flash Faults", Accepted for presentation in the 51th IEEE IAS Industrial and Commercial Power Systems Technical Conference (ICPS 2015), Calgary, AB, May 2015.
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Academic Activities

- IET Transactions on Generation, Transmission and Distribution, Reviewer since 2014.
- IEEE International Conference on Power and Energy (PECON 2014) Kuching Sarawak, Malaysia, Reviewer.
- ICCVIA2014 PATRON.UAE, Technical Committee.
- IEEE Transactions on Sustainable Energy, Reviewer since 2013.
- 48th IEEE IAS Annual Meeting 2012 Conference Orlando. FL. USA, Reviewer.
- 8th International Conference on Intelligent Information Processing (ICIIP2013) Reviewer.
- IEEE International Conference on Power and Energy (PEC), Kota Kinabalu Sabah, Malaysia, 2-5 December 2012, Reviewer.
- IEEE EPEC Electric Power and Energy Conference Canada-Halifax, 2010, Reviewer.