EFFICIENCY IMPROVEMENT

FOR SMALL-SCALE SINGLE-PHASE GRID-CONNECTED INVERTERS

by

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ABSTRACT

This Ph.D. research focuses on efficiency improvement methods for small-scale single-phase grid-connected inverters. Many attempts applied to increase inverters' efficiency found in the recent literature can be primarily summarized into two categories: specific topologies and complicated control algorithms, which result in a considerable increase in system cost and control complexity. Meanwhile, the power quality is another important issue for grid-connected inverters to comply with the utility standards. To overcome the drawbacks of the traditional methods and satisfy the utility requirement, a novel control algorithm called "variable switching frequency control (VSFC)" is developed as a major part of this thesis work to increase the overall efficiency of the inverter through selecting optimal switching frequencies of pulse width modulation (PWM) in real time while meeting requirements of grid interconnection standards. According to the inverter loss analysis and current harmonic estimation model presented in this dissertation, the selection of switching frequencies for the grid-connected inverter optimized by the proposed "VSFC" ensures that the inverter operates with maximum efficiencies at different output levels.

In addition, as the operational switching frequency applied to the inverter under "VSFC" changes along with variations of work conditions, when the inverter operates at a low or medium switching frequency, the time-delay effect caused by sampling distribution, computation of the control program in DSP and inherent PWM generator update is amplified and can severely degrade the system stability and performance. Thus, a robust current control scheme featuring high adaptability to time delays and system uncertainties

and high robustness to parameter mismatch is developed in this research. The proposed scheme is built on a structure of the predictive current controller and developed with an improved time-delay compensation technique which greatly reduces the current tracking errors through a simple weighted filter predictor (WFP) and completely eliminates static voltage errors introduced by uncertain system disturbances through a robust adaptive voltage compensator (AVC).

The developed new control methods for grid-connected inverters have been verified through computer simulations and laboratory experiments. The results of simulation and experiment investigation have demonstrated the improvements of these methods in overall inverter efficiency and performance.

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List of Abbreviations

AVC	adaptive voltage compensator
CCPWM	current-controlled PWM
CCSVPWM	current-controlled SVPWM
CEC	California Energy Commission
DFIG	doubly fed induction generator
DG	distributed generation
EMI	electromagnetic interference
ESR	equivalent series resistance
FACTS	flexible ac transmission system
FFT	fast Fourier transform
FOH	first-order hold
IGBT	insulated-gate bipolar transistor
MIC	module integrated converter
MIP	million instructions per second
MOSFET	metal oxide semiconductor field-effect transistor
MPC	model predictive control
MPPT	maximum power point tracking
PEC	power electronic converter
PF	power factor
PI	proportional-integral
PMSG	permanent magnet synchronous generator

PV	photovoltaic
PWM	pulse width modulation
RMS	root mean square
SCIG	squirrel cage induction generator
SPWM	sinusoidal pulse width modulation
SVPWM	space vector pulse width modulation
TDD	total demand distortion
THD	total harmonic distortion
TI	Texas Instruments
VSFC	variable switching frequency control
VSI	voltage source inverters
WECS	wind energy conversion system
WFP	weighted filter predictor
WRIG	wound rotor induction generator
WRSG	wound rotor synchronous generator
ZCS	zero-current-switching
ZCT	zero-current-transition
ZOH	zero-order hold
ZVS	zero-voltage-switching
ZVT	zero-voltage-transition

1 Introduction

1.1 Background

Due to the increasing energy demand and pressing environmental issues, renewable energy technologies have grown substantially over the past few years. Among the available renewable energy resources, wind and solar photovoltaic (PV) energy have been playing an increasingly important role in the renewable power generation and widely applied to distributed generation (DG) installations [1]-[4]. In particular, the small-scale (<100 kW) grid-connected wind and PV systems [5]-[9] have been significantly developed in recent years, driven by government incentives as well as the need for electricity in rural areas. According to the statistics from [10], the number of small-scale turbines installed in 2010 exceeded 656,000, globally, and total installed capacity has enjoyed an average increase of 35% annually; Solar PV capacity in operation at the end of 2011 was about 10 times as that just five years before, and the average annual growth rate exceeded 58% during the period from the end of 2006 through 2011, most of which is grid-connected [11], [12]. Inverters are the essential part of grid-connected DG systems to perform dc to ac conversions producing the high quality output.

This Ph.D. research focuses particularly on efficiency improvement methods for small-scale single-phase grid-connected inverters. As a major part of this thesis work, a novel control algorithm called “variable switching frequency control (VSFC)” is developed to increase the overall efficiency of the inverter through selecting optimal switching

frequencies in real time while meeting requirements for the grid connection. Also, an improved current controller is presented to minimize or eliminate the impacts of control delay and the variation of filter inductance.

This chapter is divided into four parts—the background information about small-scale grid-connected wind and PV generation systems as well as international standards for grid-connected inverters, literature review on efficiency improvement methods for the inverter stated in recent researches, primary objectives of the research and the organization of this dissertation.

1.2 Small-Scale Grid-Connected Wind and PV Generation Systems

The penetration of electric energy supplied from small-scale wind and solar generators into the power grid has been on sustained increase in recent years. In general, for a small-scale grid-connected generation system, generators are not connected directly to the grid. Power electronic converters are required to ensure the efficient and adaptive energy transfer from renewable resources into the power system. As for small-scale grid-connected wind and PV systems, dc/dc converters and dc/ac inverters are normally utilized as the interface between wind generators or PV panels and the grid.

1.2.1 Grid-Connected Wind Systems

With the steady development of wind power technology for the past 35 years [13]-[15], power electronics has been playing important and quite different roles in various wind

energy conversion systems (WECSs). In the 1980s, the power converters for wind turbines were simple thysistor soft starters used to limit the high inrush current produced by initially connecting the squirrel cage induction generator (SCIG) to the power grid. In this case, the power electronic device did not need to carry the power continuously [16], [17]. In the 1990s, power electronic technology was mainly used for the rotor resistance control of a wound rotor induction generator (WRIG) by adding an extra chopper-controlled resistance in the rotor circuit, whose size defines the range of variable speed of the turbine generator. Typically, the speed control range is 0-10% above the synchronous speed [18], [19]. Since 2000, the partial-scale power converter for the doubly fed induction generator (DFIG) has dominated the wind generation market with attractive characteristics of smaller power capacity and normally 30% speed control range. And then, more advanced full rating power converters were introduced to perform the full power and speed control and a better grid connection compared with the DFIG-based WECS. The generator adopted can be the asynchronous generator, wound rotor synchronous generator (WRSG) or permanent magnet synchronous generator (PMSG), dependent primarily on the rating of loads and speed of turbines [20].

In recent years, the use of PMSG-based full-rating power converters has become dominant in the field of small wind generation. As a PMSG is self-excited, there is no reactive power needed on the generator side and thus active power flows uni-directionally from the PMSG to the grid through the power converter, which allows the PMSG-based WECS to operate with a high power factor and high efficiency [21]. As well, a multi-pole design for the PMSG can be used to either totally eliminate the gear box or reduce its size.

This advantage becomes crucial for wind turbine installation in harsh environment characterized by low temperature [22], [23]. There are two typical grid-connected WECSs based on PMSGs and voltage source inverters (VSIs) which are shown in Fig. 1.1.

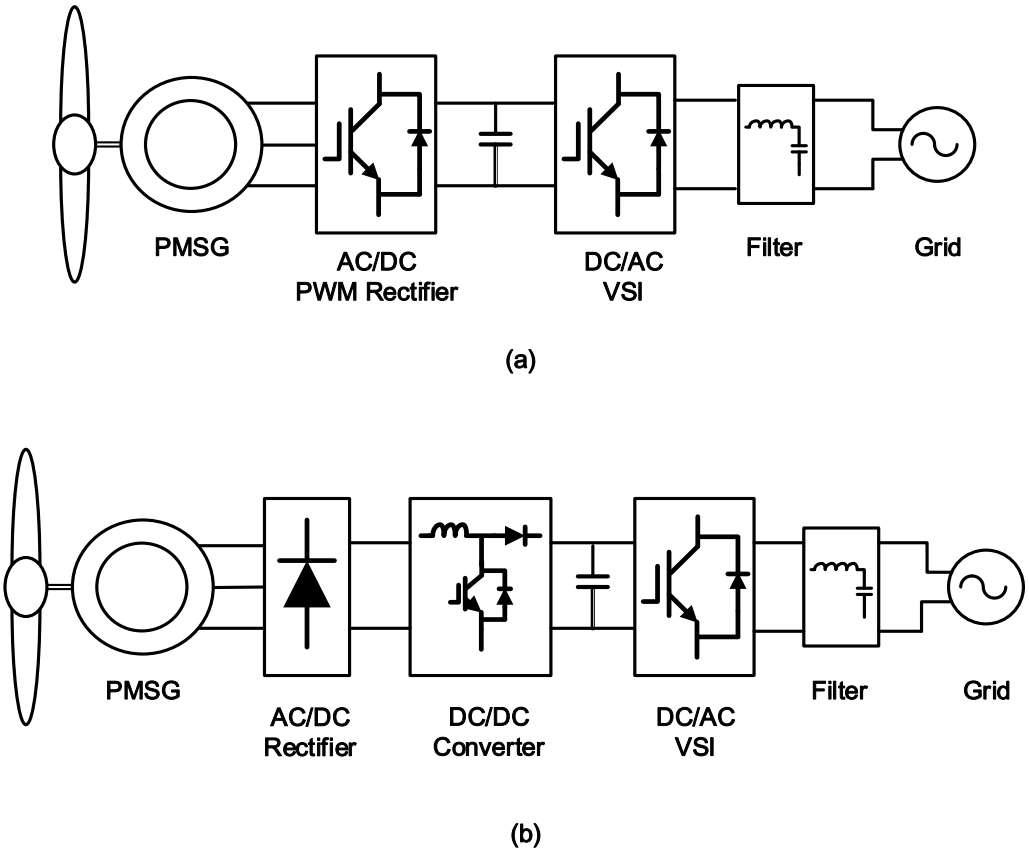


Fig. 1.1 PMSG-based WECSs (a) PMSG with back-to-back PWM converters (b) PMSG with an uncontrolled diode-rectifier and a boost converter

Fig. 1.1 (a) shows a PMSG-based WECS connected to the grid with two voltage source pulse width modulation (PWM) converters in a back-to-back structure. The generator side ac/dc converter acts as an active rectifier, while the converter connected to the grid is

used to convert dc power into grid-synchronized ac power. These two converters share the same dc link. The technical advantage of this topology is to offer a separate control of the two converters, thus affording some line fault protection as well as allowing compensation for the power imbalance between the generator side and the grid side. Both voltage control of the dc link and pitch angle control of the wind turbine are necessary.

Fig. 1.1 (b) shows a PMSG-based WECS connected to the grid through a diode-bridge rectifier, a boost dc/dc converter and a VSI. The ac power from the generator is rectified by the diode-bridge rectifier and maximum power point tracking (MPPT) for the turbine is achieved by the boost dc/dc converter [24]. The grid-connected VSI has the similar functions as in Fig. 1.1 (a). The advantage of this technique is that there is no wind speed measurement required in the system and the control for variations of parameters of the turbine or the generator can be achieved effectively by the boost converter.

1.2.2 Grid-Connected PV Systems

With low cost, high efficiency and high adaptability, single-phase grid-connected PV conversion system is playing an increasingly important role in the development of solar energy industry. In general, the topologies of PV inverters can be classified into single-stage and multi-stage depending on the number of power processing stages [25].

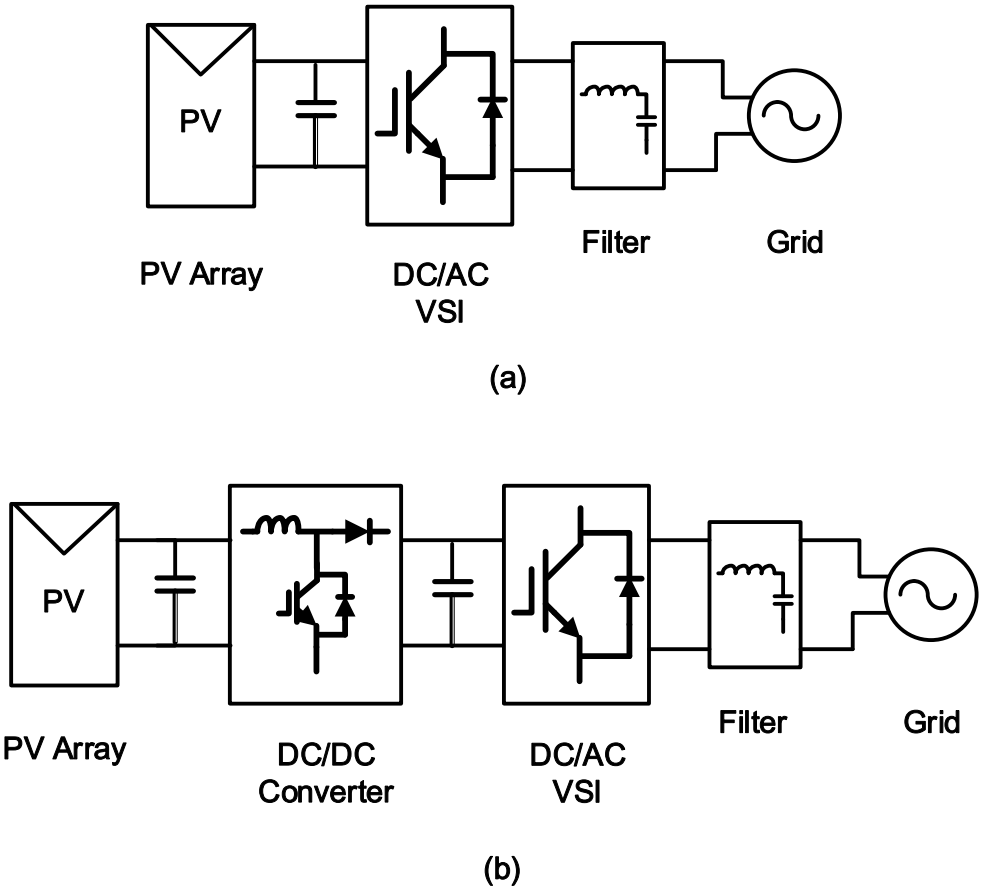


Fig. 1.2 Grid-connected PV system (a) Single-stage inverter (b) Two-stage inverter

The single-stage inverter, as shown in Fig. 1.2 (a), is defined as an inverter with only one stage of power conversion to handle all the tasks including implementing MPPT algorithm, regulating the output current fed to the grid and stepping up the low input voltage from PV arrays. Although single-stage inverters are generally high-efficient and low-cost due to the simple structure and low component counts, they usually suffer from limited power capacity and operating voltage range of PV panels [26]-[28].

Fig. 1.2 (b) shows a typical two-stage grid-connected inverter, which is widely employed in PV conversion systems. The first stage operates as a boost or buck-boost type dc to dc converter to perform the MPPT as well as voltage amplification. The second stage is used as a normal VSI. Compared with single-stage inverters, multi-stage inverters boast a wide input voltage range, a larger power capacity and easier implementation of several control functions (i.e., MPPT, reactive power compensation, etc.); however, multi-stage inverters do have some drawbacks such as bigger size, lower efficiency and higher cost [5], [29], [30].

1.3 Literature Review

The combination of modern life, economic development and industrialization around the world means that global electricity demand will continue to grow. However, the generation of electricity power worldwide today remains largely dominated by the use of fossil fuels (i.e. oil, gas and coal), which result in serious pollution threats. In order to reduce these environmental hazards while meeting the increasing electricity demands, the power production via wind and solar radiation has become a remarkable trend and has grown rapidly in the last two decades. Although technology development provides many advanced solutions in wind and solar energy exploitation, the cost is still higher than that of traditional power resources. In this context, the pursuit of greater efficiency of electricity production has been considered as key topic for both institutional research and industrial applications to pursue high and rapid return on investment.

In fact, the energy conversion efficiency of wind and solar generation systems can be improved in two distinct ways. One is to maximize wind and solar energy utilization primarily through technology development of wind turbines and PV modules as well as implementation of MPPT control algorithms. The other is to improve the efficiency of equipment related to power conversion, especially the power electronics part (i.e. power converters, grid-connected inverters and etc.). Not only does improving the efficiency of power electronics generate more power under the same environmental condition, but also makes the conversion process more reliable together with lower heat dissipation and a longer lifespan of the plant.

This section describes some typical methods to improve the efficiency of power conversion often seen in the related literature.

1.3.1 Resonant Techniques

The switching losses of a traditional PWM inverter could be a significant portion of the total power losses due to the high di/dt and dv/dt values when the power semiconductor devices are turned on and off at the load current which can result in higher electromagnetic interference (EMI) as well [31]. In order to minimize or even eliminate the disadvantages of hard-switching PWM control, several resonant techniques are proposed. The resonant inverters, which include series and parallel resonant inverters [32], [33], class E resonant inverters [34], quasi-resonant inverters [35], [36] and multi-resonant inverters [37], can work under higher switching frequency with lower switching

losses and lower electromagnetic interference by creating a LC-resonant tank or network to shape the current and voltage waveforms of semiconductor devices and thereafter achieve either zero-voltage-switching (ZVS) or zero-current-switching (ZCS).

However, due to the resonant nature of the voltage and current waveforms, the operation of resonant inverters usually involves high circulating energy, even when the load is disconnected, which leads to a substantial increase in conduction losses, thus offsetting the reduction in switching losses [35]. In addition, since resonant inverters usually operate with a variable switching frequency and the range of switching frequencies in some topologies can be very large, this kind of inverters would result in higher EMI and noises.

1.3.2 Soft-Switching PWM Techniques

Soft-switching PWM techniques are aimed at combining the advantages of both the conventional PWM techniques and the resonant techniques [38]. By incorporating the certain resonant network into a PWM scheme, the soft-switching PWM inverters including the ZVS inverters [39], the ZCS inverters [40], the zero-voltage-transition (ZVT) inverters [41] and the zero-current-transition (ZCT) inverters [42], [43] can reduce the circulating energy loss effectively while minimizing the switching loss. Meanwhile, the operation with a constant switching frequency favors the optimization of reactive components and closed-loop bandwidth as well as the filtering of EMI and noises [44].

However, the major drawbacks of soft-switching PWM inverters lie in the requirements of high rating auxiliary switches and diodes as well as possible additional resonant inductors and capacitors, both of which could increase the cost and control complexity of the inverters.

1.3.3 Transformerless Inverters

Transformerless grid-connected PV inverters proposed in [45], [46] have the advantages of higher efficiency, lower cost and smaller size compared with their counterparts with transformer galvanic isolation. However, if the isolation transformer is removed, the high-frequency common-mode voltage may induce a large leakage current flowing through the inverter to the ground. The leakage current will cause problems including higher system losses, lower quality of the grid current, possible introductions of EMI and even serious safety issues.

In order to eliminate the leakage current from the transformerless inverter applications, the common-mode voltage has to be kept constant during all operation modes. Employing a bipolar sinusoidal pulse width modulation (SPWM) technique for the half-bridge inverter or the full-bridge inverter is a simple way to avoid variations of the common-mode voltage, but both of the current ripples across the filters and the switching losses are large [47].

1.3.4 Multilevel Inverters

Although multilevel inverter has always been considered as an attractive solution in high voltage and high current applications [48]-[50], such as utility interface for renewable energy systems [51] and flexible ac transmission system (FACTS) devices [52], along with the development of low-voltage power semiconductors (e.g. SiC diode), more applications of multilevel inverters have been extended from high to low voltage range (<1000 V) recently [53]-[55]. Compared with traditional two-level inverters, multilevel inverters have the advantages of lower voltage stress across power devices, better output quality, smaller size of the filters and a higher efficiency.

However, the involvement of a large quantity of power switches leads to a considerable increase in both control complexity and the cost of the overall system.

1.3.5 Module Integrated Converter (MIC)

PV MICs receive a great deal of research attention recently in grid-connected solar generation field [56]-[58] due to their distinctive features of flexible panel-level MPPT control and high system-level conversion efficiency. Compared with traditional string/centralized PV inverters suffering from the mismatch of output characteristics among PV modules [59], MICs implement individual MPPT algorithm to assure that each module operates at its own maximum power point. Thus, the grid-connected PV system with MICs has advantages of efficient energy harvesting and simple scalability

[60]. However, MICs as front-end dc/dc converters for grid-connected inverters increase cost and control complexity of the plant.

1.3.6 Hysteresis Control Method

The hysteresis control technique has been proven to be a suitable solution for all the applications of current-controlled VSIs with characteristics of simplicity, low switching losses and excellent dynamic performance [61]. The main drawback of the hysteresis current control is the unpredictable switching frequencies of the inverter with a wide range of possible values, which leads to worse harmonic performance and larger size of filters.

1.3.7 Other PWM Algorithms

PWM techniques such as discontinuous PWM methods [62], [63] or near-state PWM methods [64] also have severe impacts on the inverter switching losses, and most of them are not capable of decreasing switching losses for the single-phase inverter; in addition, the possible introduction of high frequency harmonic components could become an issue in the output [65]. [66] proposed a SPWM-based variable switching frequency scheme to minimize the total switching losses of a single-phase inverter; however, the requirement of a rigorous model of the ripple current and huge off-line calculation burden make the algorithm endowed with poor robustness and dynamic response performance.

As a matter of fact, many attempts discussed above which have been applied to increase inverters' efficiency can be summarized into two categories: modified topology and complicated control algorithm. The former needs additional electronic components and thus increasing the cost and control complexity of the overall system; whereas for the latter, it is hard to satisfy the requirements for both higher efficiency and better output power quality.

1.4 Research Objectives and Methodologies

1.4.1 Problem Overview

As discussed in the previous section, the efficiency of power conversion which affects system reliability and the payback period on investments is considered as a key factor to evaluate the performance of grid-connected wind or PV generation systems. However, as for the methods employed to improve the efficiency of power conversion equipment, most of them are particular to specific energy resources or schematics. Thus, finding an effective way to improve the efficiency for power converters is the main concern of this Ph.D. research.

The other problem is power quality control. Since the generation system is connected to the grid, grid interconnection standards must be followed [67]. The typical international standards include IEEE 1547 [68], UL 1741 [69] and AS 4777 [70], which deal with issues including power quality, grid protection requirement, etc. The current Total Harmonic Distortion (THD) and the current Total Demand Distortion (TDD), two of

most important performance requirements for the quality of the injected grid current, are limited to a 5% allowance by the standards AS 4777 and IEEE 1547, respectively. Therefore, a good current controller integrated with the efficiency improvement algorithm is required for the grid-connected inverter to guarantee the compliance with the power quality requirements of international interconnection standards.

1.4.2 Research Objectives

In order to provide the solution to problems discussed above, three main research objectives are set and achieved in this thesis.

The first objective of this Ph.D. research is to build a mathematical model of output current ripples which can be used to estimate the THD or TDD performance of the grid output current with different inputs and control algorithms applied.

The second objective is to develop a novel control scheme, called VSFC, to minimize the total switching loss of the inverter within the different operation conditions as well as to meet THD or TDD requirement for the output current feeding into the grid.

The third objective is to improve the predictive current control algorithm which is implemented by the grid-connected inverter to minimize or eliminate the impacts of control delays and variations of the filter inductance.

1.4.3 Research Methodologies

Grid-connected inverter is the most important and essential element in various small-scale wind and PV generation systems. Improving the efficiency of the inverter can be viewed as the direct and effective way to boost the whole efficiency of the energy conversion process. Therefore, a detailed loss analysis of the inverter has been identified as the first step of this research. The loss analysis lays a foundation for finding out the main factors which make the energy losses and affect the efficiency.

The second step is to establish the THD and TDD models of output grid current. For grid-connected inverters, the harmonic distortion of the output current is the main performance factor under consideration of satisfying a THD or TDD requirement according to the standard AS 4777 or IEEE 1547. Since current harmonic performance is intimately related to the inverter switching frequency and normally higher switching frequency results in lower THD or TDD of the output current [16], the THD and TDD models based on output current ripples should be built to select the optimal switching frequencies at different output levels complied by grid interconnection requirements.

The last step is to explore a variable switching frequency control algorithm to improve the efficiency of the inverter while meeting a THD or TDD requirement specified by grid interconnection standards. Based on the analysis from the first two steps, selecting an optimal switching frequency of the inverter can be considered as an effective way to improve the efficiency as a result of tradeoff between reducing the switching losses and lowering a THD or TDD performance of output current. In addition, both a novel

sampling strategy and an improved current controller are developed to satisfy the requirement for the digital control of the proposed algorithm. The sampling system is applied to ensure that the variable switching frequency control works properly under the condition that the sampling points are randomly distributed in a PWM period when the switching frequency is changed. While the current controller is improved to compensate the impact of inevasible control delay of a digital system as well as enhance robustness of the plant against parameter variations. The efficiency improvement with the proposed variable switching frequency control can be verified by both a Matlab-based simulation and an experimental platform of a 10 kW single-phase grid-connected inverter.

1.5 Organization of the Dissertation

This Ph.D. dissertation is organized into the following six chapters.

Chapter 1 as an introductory section presents background information about grid-connected wind and PV generation systems, reviews of recent literature on improving the efficiency of inverters, and research objectives of this Ph.D. thesis.

Chapter 2 details the system configuration, PWM control methods and loss analysis of a single-phase grid-connected inverter. Matlab-based simulation results show the efficiency performance of inverters with different control algorithms. In addition, the influence of switching frequency on the inverter's loss distribution is discussed.

In Chapter 3, a THD or TDD model of the grid current is established. In fact, the output grid current can be seen as the superposition of the fundamental current and current ripples. The relationship between the THD or TDD model and the switching frequency has been clarified by the estimation of current ripples.

In Chapter 4, a novel control algorithm is explored to improve the efficiency for a general single-phase grid-connected inverter. The proposed method reduces the switching losses of an inverter through selecting an optimal switching frequency in real time with different inputs. Meanwhile, the output power quality can be guaranteed to meet the THD or TDD requirement for grid interconnection standards. Related simulation and experimental results have also been presented in this chapter.

In Chapter 5, an improved current controller is developed and problems caused by control delays and uncertain system disturbances are discussed. Also, the description and design of this current controller is detailed in this chapter. Not only does the developed controller minimizes the impact of delay issues, but also enhances robustness of the system, which is verified by a series of tests with the filter inductance varying.

Chapter 6 as a brief summary of the dissertation states the conclusions and main contributions of this Ph. D. research, as well as offers recommendations for the future research on related topics.

2 Efficiency Model of Single-Phase Grid-Connected Inverters

2.1 Introduction

This chapter addresses the power loss distribution in single-phase grid-connected VSIs. At the beginning, system configurations are introduced. DC-link capacitors are used as an energy buffer against the mismatch between the power generated from wind turbines or PV arrays and the power fed into the utility grid. An average dc-link voltage control scheme is proposed to smooth this power fluctuation. Then, three PWM techniques for the insulated-gate bipolar transistor (IGBT)-based full-bridge inverter, including uniform PWM control, SPWM control and double-frequency space vector PWM (SVPWM) control, are discussed and analyzed.

In addition, analytical expressions of VSI losses are presented in this chapter. An M-language-based simulation is proposed to establish the efficiency model of VSIs and then compare efficiencies under the different operation conditions. Experimental results verify the accuracy of the efficiency model.

2.2 Single-Phase Grid-Connected VSIs

2.2.1 System Descriptions

As discussed in Section 1.2, single-phase inverters as an essential part of small-scale grid-connected wind and PV generation systems fulfill a variety of functions, which can be summarized as follows.

a) DC-ac power conversion: This function is to change a dc input voltage to a symmetric ac output voltage of the desired voltage and frequency of the utility grid using controlled power semiconductor devices [71], such as metal oxide semiconductor field-effect transistors (MOSFETs), IGBTs and etc. Generally, an output voltage can be produced by PWM control within the inverter when the dc input voltage is fixed and not controllable [31].

b) Energy flow control: The dc-link consists of electrolytic capacitors, film capacitors or batteries which act as an energy buffer to provide the difference between the output power of the front-end generators and the input power of the inverters. Thus, with a proper dc-link voltage control scheme, the regulation of the dc-link voltage can be achieved and the output power of the inverter is optimized.

c) Output power quality assurances: Due to the nature of renewable energy, the controllability or lack of it is the main drawback of the distributed wind or PV generation systems, resulting in grid instability or even failure [72]. Thus, the power fed to the utility grid needs to be regulated by effective control of inverters to achieve the power quality requirements of standards for interconnecting distributed resources with electric power systems. The main performance of power quality includes harmonic distortion of the grid current and voltage, power factor, frequency deviation and etc.

d) DG systems protection: Grid-connected inverters provide an overall solution to inject the power generated from DG systems into the grid that includes protection against abnormal voltage, current, frequency and temperature conditions in the

process of generation as well as the possible damage to people or equipment, such as anti-islanding protection and electrical isolation [31].

e) Specific objective realization: Some specific functions can be accomplished by integrating certain algorithm into inverters, such as MPPT methods or reactive power compensation.

Fig. 2.1 presents a typical topology of single-phase grid-connected VSIs which is employed for this Ph.D. research. It is composed of a dc voltage source generated from wind turbines or PV arrays directly or indirectly which can be seen in Fig. 1.1 and Fig. 1.2, a dc-link capacitor bank used as an energy buffer, and a single-phase full-bridge IGBT-inverter with an L filter.

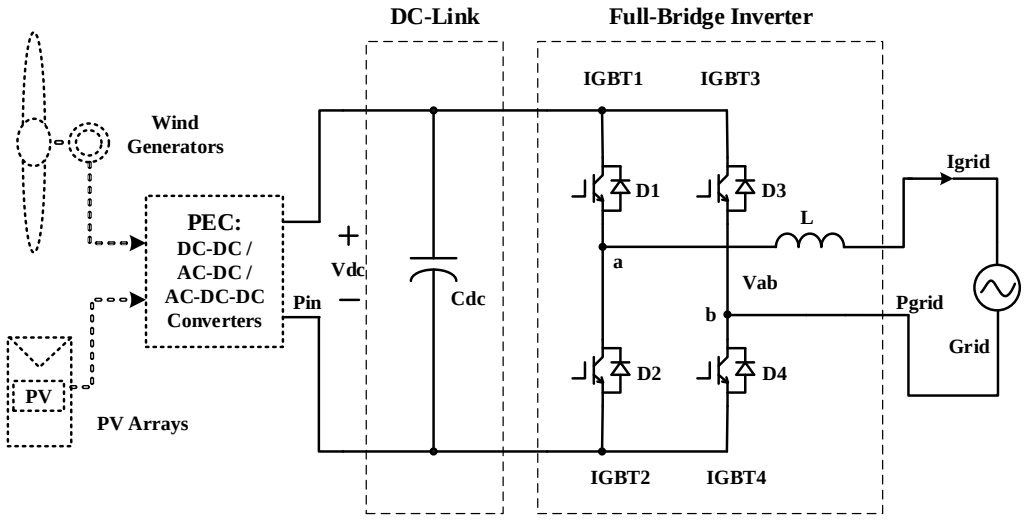


Fig. 2.1 Typical topology of a single-phase grid-connected VSI

The VSI is normally preceded by a set of extraction and generation apparatus for renewable wind and solar energy [73], as shown with dotted lines in Fig. 2.1. The dc source of the proposed VSI is obtained from the output of front-end power electronic converters (PECs) which can operate with MPPT functions for the renewable energy sources. When connecting to PV arrays, typical dc-dc converters are used [60], while for wind generation systems PECs are generally featured in ac-dc topologies [74], [75] or ac-dc-dc topologies [76]. The PEC is connected to the dc-link of the VSI, whose capacitors are used to reduce the dc-link voltage ripple as well as decouple the power between the PEC output and input of the full-bridge inverter. The high quality power output can be accomplished with the full-bridge inverter with proper PWM techniques when connecting to the grid.

2.2.2 DC-Link Analysis

As discussed above, dc-link plays an important role in linking full-bridge inverters with various front-end PECs. Electrolytic capacitors of the dc-link are used to balance the power flow against the power mismatch between the output of PECs and the input of full-bridge inverters with proposed constant dc-link voltage control, as well as to reduce the inherent double-line-frequency ripples (refer to Equation (2.15)) with their large capacitance per unit volume. Fig. 2.2 shows a typical dc-link voltage waveforms which can be seen as a combination of a constant dc voltage and a double-line frequency ripple voltage component.

A. Average DC-Link Voltage Control

There are two main factors that influence a voltage variation of the dc-link. The first one is the power mismatch. As shown in Fig. 2.1, the power being transferred from a front-end PEC into the full-bridge inverter charges the dc-link capacitors first and increases their voltage. If energy stored in the capacitors is not released by the full-bridge inverter in a timely manner, the capacitor voltage will continue to increase until capacitors are permanent damaged. Conversely, if the demand power for the full-bridge inverter is too much, the voltage of capacitors on the dc-link will decrease. In other words, if the input power of the dc-link from a PEC p_{in} is greater than the output power to the grid p_{grid}, then the dc-link voltage will increase; on the contrary, if p_{in} is lower than p_{grid}, the dc-link voltage will decrease. Thus, a constant dc-link voltage can be considered as an indication that the power flow through the system is balanced. Here, the dc-link plays a role of an energy buffer to provide the power difference between p_{in} and p_{grid}. Assuming a lossless system for simplicity, the instantaneous power of the dc-link is given by

$$p_{dc} = p_{in} - p_{grid} \tag{2.1}$$

However, as the change of the power from PECs for wind and PV generation applications is relatively slow [77], we assume that the power p_{in} and p_{grid} remain constant in a cycle of the grid voltage. Thus, (2.1) can be rewritten as

$$\overline{P_{dc}} = \overline{P_{in}} - \overline{P_{grid}} \tag{2.2}$$

where the bar denotes the average value.

Therefore, an average dc-link voltage control strategy is proposed to regulate $\overline{P_{grid}}$ to match $\overline{P_{in}}$ through monitoring the voltage difference between the average of dc-link voltage measurement and a preset average reference value (shown as the green dotted line in Fig. 2.2). The control system is shown in Fig. 2.3.

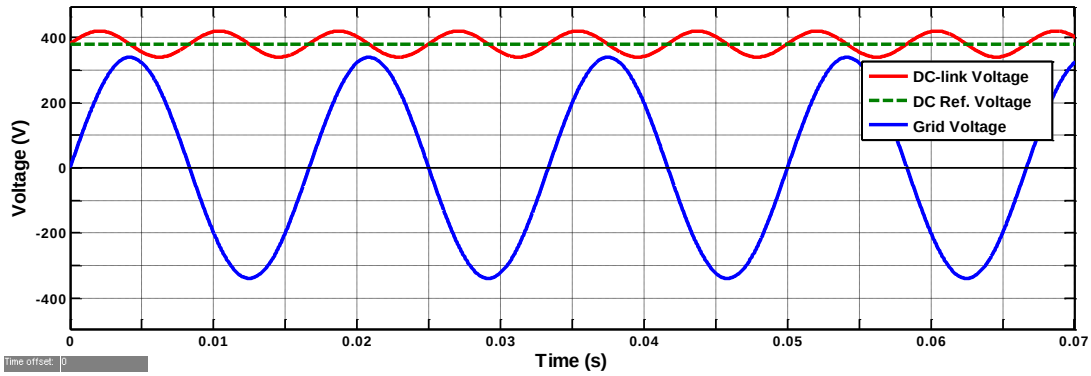


Fig. 2.2 Typical waveforms of single-phase grid-connected VSIs

According to the difference between the measurement and reference values of the average dc-link voltage, a Proportional-Integral (PI) controller is implemented to yield the amplitude of the reference current I_{ref} for the full-bridge inverter. The PI current controller $G_{dc}(s)$ is defined as

$$G_{dc}(s) = K_p + \frac{K_i}{s} \tag{2.3}$$

where K_p and K_i are the proportional and integral gains, respectively.

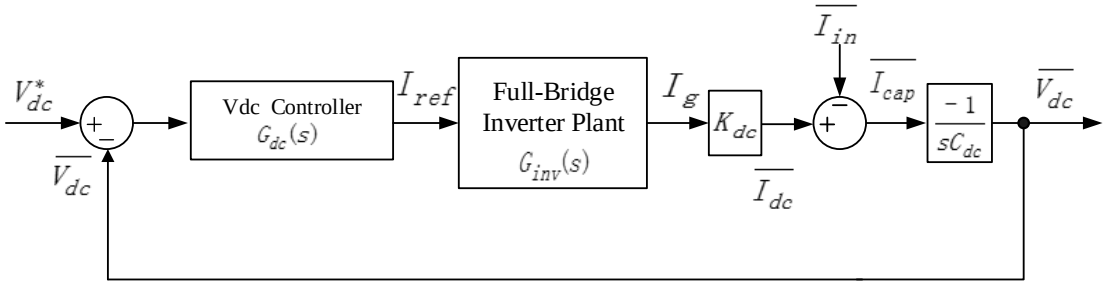


Fig. 2.3 Constant dc-link voltage control system

The block diagrams of full-bridge inverter plants can be represented differently due to distinctive control methods and hardware structures of inverters, but the gain of the transfer function of the plants G_{inv} should approximately equal to one when the proper current control algorithms are applied to, which can be expressed as

$$|G_{inv}(s)| \approx 1 \tag{2.4}$$

In this dissertation, a current-controlled PWM (CCPWM) strategy is employed to achieve high performance of the output grid current and an averaged switch model [78] is used to describe the operation of the inverter. The block diagram of the inverter control is shown in Fig. 2.4 and a detailed analysis is presented in Chapter 4.

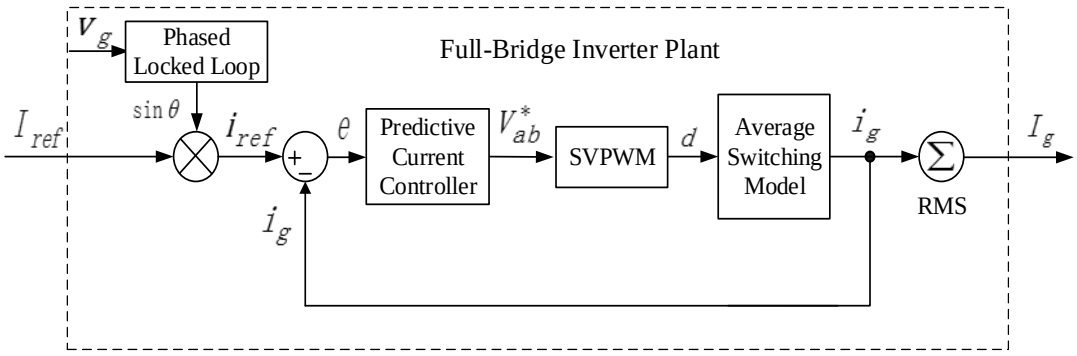


Fig. 2.4 Control diagram of the full-bridge inverter

The transfer function K_{dc} shown in Fig. 2.3 is used to characterize the relationship between the root mean square (RMS) values of the grid current and the average current of the dc bus $\overline{I_{dc}}$. Fig. 2.5 shows the equivalent circuit of the average dc-link model. The current $\overline{I_{in}}$ corresponds to the power injected from front-end PECs and $\overline{I_{cap}}$ refers to the average current flowing in dc-link capacitors. Thus, the circuit of the dc-link can be expressed using the current balancing equation as

$$\overline{I_{in}} = \overline{I_{dc}} + \overline{I_{cap}} \tag{2.5}$$

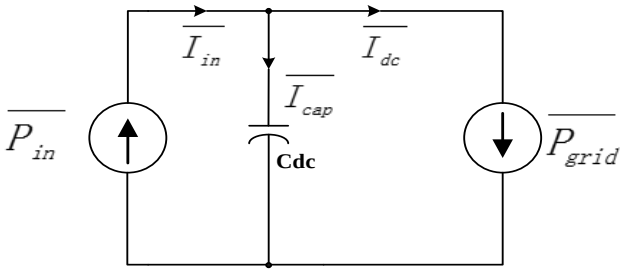


Fig. 2.5 DC-link equivalent circuit

Supposing that the voltage of the dc-link remains a constant during a cycle of the grid voltage and is represented by the average voltage $\overline{V_{dc}}$, when neglecting the capacitor losses, the current equation can be obtained based on (2.2) as

$$\overline{I_{in}} = \frac{\overline{P_{grid}}+\overline{P_{dc}}}{\overline{V_{dc}}} = \frac{V_g I_g}{\overline{V_{dc}}} + \overline{I_{cap}} \tag{2.6}$$

where V_g and I_g are RMS values of the grid voltage and current, respectively, and $V_g I_g$ is used to represent the average power of the grid, $\overline{P_{grid}}$, for single-phase VSIs.

Combining (2.6) with (2.5) yields

$$\overline{I_{dc}} = \frac{V_g}{\overline{V_{dc}}} I_g \tag{2.7}$$

where $\frac{V_g}{\overline{V_{dc}}}$ can be defined as the transfer function of K_{dc}.

According to the control scheme shown in Fig. 2.3, the closed-loop transfer function of the dc-link voltage controller can be expressed as

$$\frac{V_{dc}(s)}{V_{dc}^*(s)} = \frac{-K_{dc}K_p s - K_{dc}K_i}{C_{dc}s^2 - K_{dc}K_p s - K_{dc}K_i} \tag{2.8}$$

Therefore, a voltage PI controller can be developed with appropriate design of parameters K_p and K_i to enforce the average output grid power $\overline{P_{grid}}$ to track the average input power $\overline{P_{in}}$ through regulating the magnitude of the reference grid current I_{ref}. Meanwhile, the average dc-link voltage is stabilized at a preset reference value of V_{dc}^*, only when

$$\overline{P_{grid}} = \overline{P_{in}} \tag{2.9}$$

B. Double-Line Frequency Voltage Ripples

The other factor resulting in voltage ripples of the dc-link is referred to as the ac fluctuation component of dc voltage caused by instantaneous output power of an inverter. Suppose that the unit power factor (PF) is realized on the output grid power, then the grid voltage and the grid current can be expressed as

$$v_g = \sqrt{2}V_g \sin(\omega t) \tag{2.10}$$

$$i_g = \sqrt{2}I_g \sin(\omega t) \tag{2.11}$$

where ω is the angular frequency of the grid voltage and t is time. Then the instantaneous output power of a single-phase VSI can be obtained as

$$p_g = 2V_g I_g \sin^2(\omega t) = V_g I_g(1 - \cos(2\,\omega t)) \tag{2.12}$$

As previously stated, $V_g I_g$ is equal to the average power of the grid, thus (2.8) can be rewritten to be

$$p_g = V_g I_g - V_g I_g \cos(2\,\omega t) = \overline{P_{grid}} - \overline{P_{grid}} \cos(2\,\omega t) \tag{2.13}$$

From (2.13), it is clear that the instantaneous grid power can be divided into a constant component $\overline{P_{grid}}$ and a power pulsation with twice the grid frequency. This pulsating power appears on the dc bus and results in the dc voltage fluctuation, which can be absorbed by large electrolytic capacitors of the dc-link.

Recall that the input power of the inverter can be seen as a constant compared with the rapidly fluctuating of the grid power p_g, hence p_{in} can be assumed equal to $\overline{P_{in}}$.

Thus, when the system operates in steady state, combine (2.9) and (2.13) with (2.1) to yield

$$p_{dc} = \overline{P_{grid}} \cos(2\,\omega t) \tag{2.14}$$

Based on the differential equation for the current flowing through the dc-link capacitors, (2.14) can be rewritten as

$$C_{dc} v_{dc} \frac{dv_{dc}}{dt} = \overline{P_{grid}} \cos(2\,\omega t) \tag{2.15}$$

where C_{dc} is the capacitance of electrolytic capacitors connected to the dc-link and v_{dc} refers to the instantaneous voltage of the dc-link capacitors.

Considering that the magnitude of the voltage ripple is much smaller than that of the average dc-link voltage, (2.15) can be simplified as

$$C_{dc}\overline{V_{dc}} \frac{dv_{dc}}{dt} \approx \overline{P_{grid}} \cos(2\,\omega t) \tag{2.16}$$

where $\overline{V_{dc}}$ is the average dc-link voltage. When the power flow through the system is balanced, $\overline{V_{dc}}$ should equal to the reference dc voltage V_{dc}^{*} with the proposed average dc-link voltage control.

Solve (2.16) to obtain

$$v_{dc} = \overline{V_{dc}} + \frac{\overline{P_{grid}}}{2\omega C_{dc}\overline{V_{dc}}} \sin(2\omega t) \tag{2.17}$$

(2.17) illustrates that the magnitude of the voltage ripple is $\frac{\overline{P_{grid}}}{2\omega C_{dc}\overline{V_{dc}}}$, which is limited by the capacitance of the dc-link capacitors. Therefore, with a given maximum magnitude of the allowed ripple voltage $V_{dc\_ripple}^{max}$, the required capacitance of dc-link capacitors can be obtained by

$$C_{dc} = \frac{\overline{P_{grid}}}{2\omega\overline{V_{dc}}V_{dc\_ripple}^{max}} \tag{2.18}$$

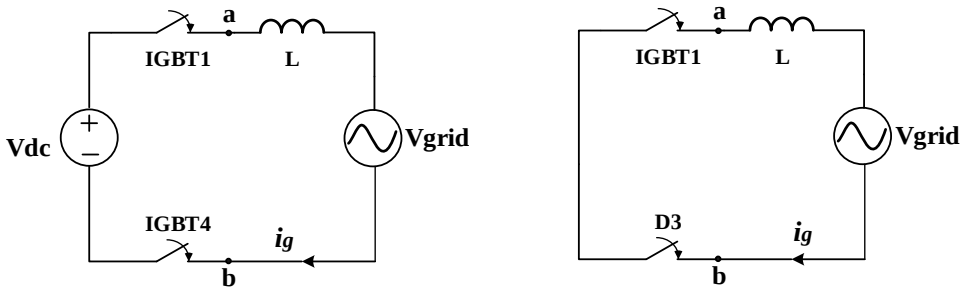
2.2.3 Operation of Full-Bridge Inverters

The topology of the full-bridge inverter investigated in this dissertation consists of four switching devices (IGBTs), four diodes and a filter inductor, shown in Fig. 2.1. The inverter operates in four modes to complete dc to ac conversion feeding power to the grid: Mode 1 and Mode 2 are in the positive half cycle of the grid voltage, while Mode 3 and Mode 4 are in the negative cycle of the grid voltage. Table 2.1 shows the operation modes of a single-phase full-bridge inverter. v_{ab} and v_{dc} represent the output voltage of the inverter and the dc-link voltage, respectively.

Table 2.1 Operation modes of a single-phase full-bridge inverter

Operation Mode	v_{ab}	Inverter operations
1	v_{dc}	IGBT1 and IGBT4 are on; IGBT2 and IGBT3 are off
2	0	IGBT1 and D3 are on; IGBT2, IGBT3 and IGBT 4 are off
3	$-v_{dc}$	IGBT2 and IGBT3 are on; IGBT1 and IGBT4 are off
4	0	IGBT2 and D4 are on; IGBT1, IGBT3 and IGBT 4 are off

During Mode 1, IGBT1 and IGBT4 are turned on simultaneously. The output voltage of the inverter (v_{ab}) is the voltage across the dc-link, v_{dc}. During Mode 2, IGBT 4 is turned off, but the load current, i_g, can continue to flow through diode D3, IGBT1, the filter inductor and the grid. Thus, v_{ab} is zero during this mode. The equivalent circuits for these two modes are shown in Fig. 2.6.



(a) Mode 1 **(b) Mode 2**

Fig. 2.6 Equivalent circuit of full-bridge inverters in the positive half cycle of the grid voltage (a) Mode 1 (b) Mode 2

Similarly, the operation of the inverter in the negative cycle can also be divided into two modes. The equivalent circuits of the inverter in Mode 3 and Mode 4 are shown in Fig. 2.7 (a) and (b), respectively. During Mode 3, both IGBT2 and IGBT 3 are turned on. The output voltage of the inverter is -v_{dc}. With IGBT2 and D4 on, v_{ab} is zero during Mode 4.

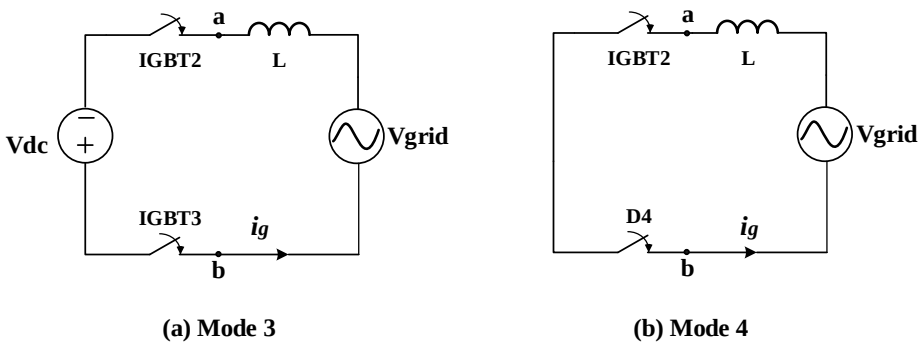


Fig. 2.7 Equivalent circuit of full-bridge inverters in the negative half cycle of the grid voltage (a) Mode 3 (b) Mode 4

In most industrial applications, the operation of the IGBTs is driven by various voltage PWM schemes which are always seen as the most efficient method to regulate the output voltage of inverters. However, for grid-connected VSIs, the output voltage and frequency are determined by the grid, thus the performance of the output current is the main concern of this research. In order to satisfy the requirement of harmonic current distortion, current control algorithms, such as CCPWM or Current-Controlled SVPWM (CCSVPWM), can be employed to control the inverter with advantages of accurate current tracking and fast dynamic response.

2.2.4 Electrical Parameters

Table 2.2 shows the electrical parameters of the single-phase grid-connected VSI under this Ph.D. research.

Table 2.2 Electrical parameters of the proposed VSI

Parameter	Value
Rated power of the VSI	10 kW
Reference dc-link voltage (V_{dc}^{*})	390 V
DC-link capacitors (C_{dc})	2050 μF
Output inductor (L)	1.6 mH
Grid voltage (V_g)	240 V
Grid frequency (f_0)	60 Hz

2.3 Loss Analysis of VSIs

2.3.1 Averaged Switch Model of VSIs

A study of the component level power losses of a VSI is presented in this section. For analyzing the expected losses, the averaged switch modeling approach [78] is used to build a complete time-invariant averaged circuit model of grid-connected VSIs. Fig. 2.8 and 2.9 shows the equivalent circuit and the typical operational waveforms of the VSI, respectively. Based on the equivalent circuits of the VSI, the model of the inverter can be obtained as

$$v_{ab} = L\frac{di_g}{dt} + v_g \tag{2.19}$$

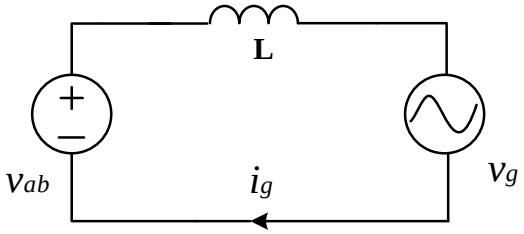


Fig. 2.8 Equivalent circuit of the VSI

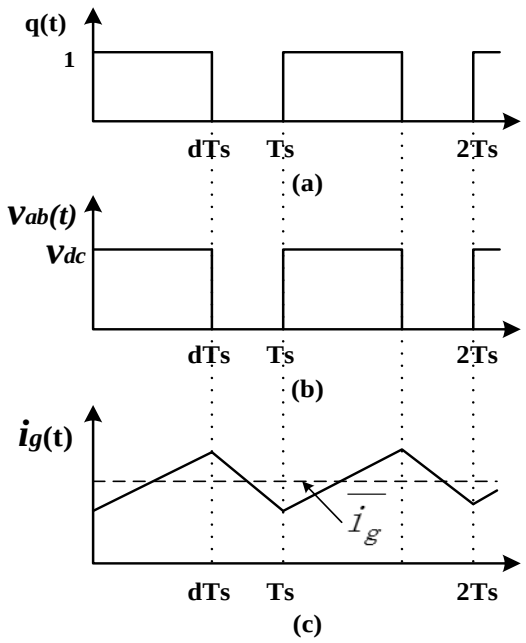


Fig. 2.9 Typical operational waveforms of the VSI (a) switching function (b) output voltage of the inverter (c) grid current

Meanwhile, the output voltage of the inverter v_{ab} can be expressed as

$$v_{ab} = v_{dc}q(t) \tag{2.20}$$

where $q(t)$ is a switching function used to describe the operations of the inverter, which is defined as

$$q(t) = \begin{cases} 1, & Mode\ 1 \\ 0, & Mode\ 2\ or\ Mode\ 4 \\ -1, & Mode\ 3 \end{cases} \tag{2.21}$$

Thus, (2.19) can be rewritten as

$$v_{dc}q(t) = L\frac{di_g}{dt} + v_g \tag{2.22}$$

For PWM VSIs, the function of $q(t)$ is a periodic, with switching period T_s and duty cycle d, as show in Fig. 2.9(a). From Fig. 2.9(c), the waveform of the grid current i_g is obviously nonlinear due to the harmonics introduced by IGBTs. However, as the ripple component of the current is small and the switching frequency is much higher than the grid frequency, i_g can be linearized over one switching period by averaging the waveform. Therefore, when the input voltage of the dc-link is seen as a constant over a switching period, the averaged switch model of the grid-connected VSI can be given by

$$\overline{v_{dc}}d = L\frac{d\overline{i_g}}{dt} + \overline{v_g} \tag{2.23}$$

where duty cycle d equals to $\overline{q(t)}$ and the overhead bar denotes the local average over an interval of switching period T_s. For example, $\overline{v_{dc}}$ is obtained from

$$\overline{v_{dc}} = \frac{1}{T_s}\int_t^{t+T_s} v_{dc}(\tau)d\tau \tag{2.24}$$

2.3.2 DC-Link Capacitor Losses

Power losses of the proposed single-phase grid-connected VSI are primarily derived from components: the dc-link capacitors, IGBTs, freewheeling diodes and the inductor filter [31]. According to the averaged switch model given by (2.23), it is easy to calculate the power losses of every component over a switching period and the total power losses of the VSI can be estimated based on the loss model of each switching period and the implemented PWM technique.

Aluminum electrolytic capacitors are used to reduce the voltage ripples of the dc-link in this dissertation, whose capacitance is 2050 μF given by (2.18) with a voltage ripple allowance of 5%. The dc-link capacitor-bank is composed of ten KMH series 450V/820μF capacitors, whose specification are shown in [79]. The corresponding equivalent series resistance (ESR) model of aluminum electrolytic capacitors which allows an estimation of the thermal losses of the capacitors with a high switching frequency operation is illustrated in (2.25) [80]

$$ESR = R_0 + R_e + R_d \tag{2.25}$$

where R_0 represents an approximately constant ohmic resistance of foil, tabs and solder terminals [81] and R_e symbolizes a temperature dependent resistance which exhibits a strong negative temperature coefficient, expressed as

$$R_e(T) = R_e(T_{Base})e^{-\frac{T-T_{base}}{F}} \tag{2.26}$$

where $R_e(T_{Base})$ is a typical resistance at a base temperature of T_{Base} (20 ℃), T is the capacitor core temperature (℃) and F is a temperature sensitivity factor [82].

The third term of (2.25) R_d represents a frequency dependent resistance of the dielectric layer of the electrolytic capacitor, which is given by

$$R_d(f) = \frac{DF_{ox}}{2\pi fC} \tag{2.27}$$

where f is the switching frequency acting on the dc-link capacitors, C is the capacitance of a capacitor and DF_{ox} is the dielectric dissipation factor whose typical value for aluminum electrolytic capacitors is 0.013 [83].

Based on the aforementioned analysis, it is evident that the ESR of the aluminum electrolytic capacitor has the largest magnitude at low temperature and low frequency. However, for a given capacitance and temperature, the variation of the ESR is very low when the operation switching frequency is in a range of one kilohertz to tens of kilohertz. Thus, a maximum ESR 0.303 Ω at a temperature of 20 ℃ specified in [79] has been used to allow reasonable loss estimation for a 450v/820μF capacitor of the dc-link. Due to the total capacitance of 2050 μF implemented (two groups are in series and each group contains five capacitors in parallel), the ESR value of the whole dc-link capacitors can be calculated as

$$ESR_{dc} = \frac{2}{5} ESR_{max} = 0.1212\ \Omega \tag{2.28}$$

Meanwhile, the ripple current flowing through the capacitors can be expressed as (2.29) based on the dc-link equivalent circuit shown in Fig. 2.5.

$$i_{cap} = \begin{cases} i_{in} - |i_g|, & Mode\ 1\ or\ Mode\ 3 \\ i_{in}, & Mode\ 2\ or\ Mode\ 4 \end{cases} \tag{2.29}$$

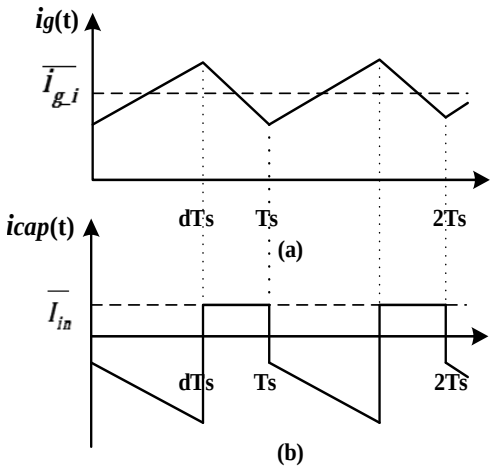


Fig. 2.10 Waveforms of the capacitor current

Fig. 2.10 shows the waveforms of the capacitor current. It is clear that the RMS capacitor ripple current is affected by the modulation technique which is implemented for the full-bridge inverter. For a given duty cycle d_i, the RMS capacitor current over the i-th switching period can be calculated by

$$I_{cap\_i\_RMS} = \sqrt{\frac{1}{T_s}\left(\int_{(i-1)T_s}^{(i-1)T_s+d_iT_s}(i_{in} - |i_g|)^2 dt + \int_{(i-1)T_s+d_iT_s}^{iT_s} {i_{in}}^2 dt\right)} \tag{2.30}$$

Considering that the input current i_{in} remains a constant during the operation and the gird current i_g is replaced with its averaged switching value $\overline{i_g}$ based on the inverter model shown in (2.23), (2.30) can be simplified as

$$\begin{aligned} I_{cap\_i\_RMS} &\approx \sqrt{\frac{1}{T_s}\left(\int_{(i-1)T_s}^{(i-1)T_s+d_iT_s}(\overline{I_{in}} - |\overline{i_{g\_i}}|)^2 dt + \int_{(i-1)T_s+d_iT_s}^{iT_s} \overline{I_{in}}^2 dt\right)} \\ &= \sqrt{\overline{I_{in}}^2 + d_i\overline{i_{g\_i}}^2 - 2d_i\overline{I_{in}}|\overline{i_{g\_i}}|} \end{aligned} \tag{2.31}$$

where $\overline{i_{g\_i}}$ refers to the average grid current during the i-th switching period

Therefore, the power losses of the dc-link capacitors can be seen as the sum of the power dissipation of every switching period which is obtained by

$$P_{cap} = \frac{1}{T_0}\sum_{i=1}^{N} {I_{cap\_i\_RMS}}^2 ESR_{dc} T_s \quad (2.32)$$

where T_0 is a period of the grid voltage and N is the total number of switching periods in T_0.

2.3.3 IGBTs and Diodes Losses

The other major contribution to the power losses of VSIs is power dissipation in semiconductor devices (IGBTs and diodes) which can be classified as conduction losses and switching losses.

A. Conduction Losses

Conduction losses result from a small voltage drop in a semiconductor device associated with the on-state due to resistance of the semiconductor material and dependent on the voltage and the temperature across the semiconductor junctions. Typically, the magnitude of the on-state voltage V_{ON} increases with the flowing current I_{ON} and is modeled by

$$V_{ON} = V_0 + R_0 I_{ON} \quad (2.33)$$

where V_0 and R_0 are coefficients from device manufacturer's specifications which are dependent on classes, ratings and operating junction temperatures of the semiconductor devices. For the proposed single-phase grid-connected inverter in this dissertation, two IGBT power modules (EUPEC BSM 100 GB 120 DN2) have been used which include

four 1200V/100A IGBTs and four build-in fast freewheeling diodes. From the module specifications [84], the on-state voltages for each IGBT and diode can be calculated as

$$V_{CE(ON)} = \begin{cases} 1 + 0.015I_{ON}, \ (V_{GE} = 15\,V, T_j = 25\,℃) \\ 1.2 + 0.019I_{ON}, \ (V_{GE} = 15\,V, T_j = 125\,℃) \end{cases} \tag{2.34}$$

$$V_{f(ON)} = \begin{cases} 1.3 + 0.01I_f, \ (V_{GE} = 0\,V, T_j = 25\,℃) \\ 0.8 + 0.01I_f, \ (V_{GE} = 0\,V, T_j = 125\,℃) \end{cases} \tag{2.35}$$

where $V_{CE(ON)}$ and $V_{f(ON)}$ are the on-state voltages of IGBTs and diodes, respectively, I_f is the current flowing through the diode, V_{GE} is the gate threshold voltage dependent on the driver circuit design and T_j is the junction temperature of the module. Assuming the on-state voltage is linearly proportional to the junction temperature in the range from 25 ℃ to 125 ℃, (2.34) and (2.35) can be simplified to

$$V_{CE(ON)} = 1 + 0.015I_{ON} + \frac{0.2+0.004I_{ON}}{100}(T_j - 25) \tag{2.36}$$

$$V_{f(ON)} = 1.3 + 0.01I_f - 0.005\big(T_j - 25\big) \tag{2.37}$$

where T_j is the actual operating junction temperature.

In order to further simplify the calculation of conduction losses, the switching behaviors such as the rise time, fall time, and delay time of IGBTs and the reverse recovery time of diodes, are neglected. Thus, the conduction losses of IGBTs and diodes of each switching period can be obtained by

$$E_{IGBT(ON)\_i} = V_{CE(ON)}\big|\overline{i_{g\_i}}\big|T_s(d_{IGBT1\_i} + d_{IGBT2\_i} + d_{IGBT3\_i} + d_{IGBT4\_i}) \tag{2.38}$$

$$E_{Diode(ON)\_i} = V_{f(ON)}\big|\overline{i_{g\_i}}\big|T_s(d_{D1\_i} + d_{D2\_i} + d_{D3\_i} + d_{D4\_i}) \tag{2.39}$$

where d_{X_i} represent the duty cycle of the semiconductor device x (shown in Fig. 2.1) in the i-th switching period.

B. Switching Losses

Switching losses are produced as a result of a simultaneous exposure of an IGBT to high voltage and current transits during every turn-on or turn-off process. Fig. 2.11 shows a typical characteristic of switching energies E_{SW_ON} and E_{SW_OFF} specified in [84] when the IGBT operates with $V_{GE} = \pm 15\,V$ and $V_{CE} = 600\,V$. For simplicity, it is assumed that the switching losses are proportional to the applied dc voltage. Therefore, the switching losses of each IGBT during one switching period E_{SW_i} can be formulated as

$$\begin{cases} E_{SW\_ON\_i} = \frac{V_{dc}}{V_{CE}}(2.5 + 0.12|\overline{i_{g\_i}}|) \times 10^{-3} \\ E_{SW\_OFF\_i} = \frac{V_{dc}}{V_{CE}}(1.8 + 0.09|\overline{i_{g\_i}}|) \times 10^{-3} \\ E_{SW\_i} = E_{SW\_ON\_i} + E_{SW\_OFF\_i} \end{cases} \tag{2.40}$$

where V_{dc} is the average dc-link voltage and suppose that $V_{dc} = constant$ with proper dc-link voltage control.

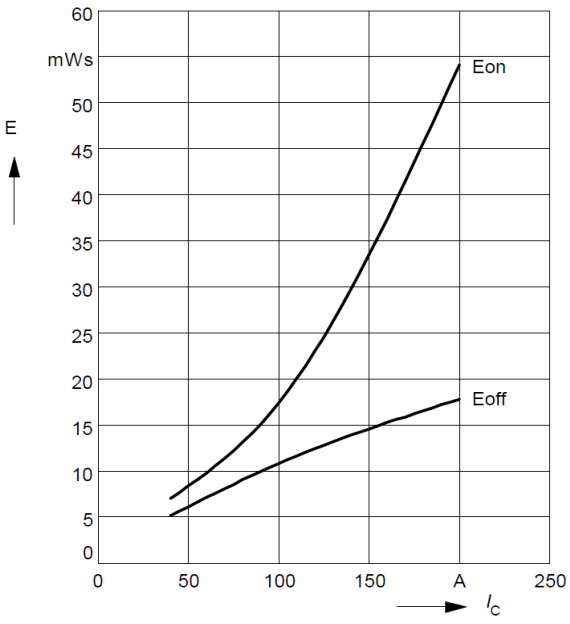


Fig. 2.11 Typical switching losses

According to (2.36), (2.37) and (2.40), the power losses of IGBTs and diodes can be derived by summing the switching energy of all switching periods in a grid period

$$P_{IGBT} = \frac{1}{T_0}\sum_{i=1}^{N}(E_{IGBT(ON)\_i} + N_{equ}E_{SW\_i}) \tag{2.41}$$

$$P_{Diode} = \frac{1}{T_0}\sum_{i=1}^{N} E_{Diode(ON)\_i} \tag{2.42}$$

where $N = \frac{T_0}{T_s}$, and N_{equ} represents the number of IGBTs that switch on and off in a switching period.

2.3.4 Filter Inductor Losses

For single-phase grid-connected VSIs, L-type filters are widely used to reduce the harmonics in generated current caused by high switching frequency operation of inverters with the advantage of simple design [85], [86]. Although the size of filter inductor is reduced along with high frequency switching, the power loss still cannot be ignored. Thus, estimation of filter inductor losses plays an important role in the efficiency evaluation of the VSI. Losses in the inductor shown in Fig. 2.1 include the copper losses and the iron losses.

The copper loss occurs due to the resistance of the copper windings of the inductor and scales with the square of the RMS grid current, which is given by

$$P_{cu} = {I_g}^2 R_{cu} \tag{2.43}$$

where I_g is the RMS grid current and R_{cu} is the resistance of the winding conductor.

The iron loss is produced in magnetic materials and primarily comprises three parts: hysteresis power loss P_{hyst}, classical eddy current loss P_{eddy} and excess loss P_{exc}, which can be expressed by employing the *Bertotti* separation model [87]:

$$P_{core} = P_{hyst} + P_{eddy} + P_{exc} \tag{2.44}$$

where the hysteresis loss P_{hyst} is the power consumed in magnetic materials during the magnetized or demagnetized process. The classical eddy current loss P_{eddy} refers to the losses due to the presence of the eddy current in the conductor materials. And as for the excess loss P_{exc}, it is interpreted in [88] and caused by the skin effect occurring in the eddy current path [89]. As the skin effect is typically observed in magnetic materials in a high frequency range over 100 kHz [90], it is assumed that the excess loss can be neglected in this dissertation, and thus the iron loss model of the proposed filter inductor can be expressed as [91], [92]

$$P_{core} = P_{hyst} + P_{eddy} = VK_h f_0 {B_m}^x + VK_{cl} f_0 \int_0^{T_0} (\frac{dB(t)}{dt})^2 \tag{2.45}$$

where V is the volume of the core, B_m is the peak flux density, f_0 is the grid frequency and the coefficients of K_h, K_{cl} and x are the parameters principally determined by the magnetic material of the core.

Assuming that the effect of the voltage harmonics on the iron loss is minor and can be neglected, the peak value of the flux density can be obtained based on Faraday's law [78], which is given by

$$\mathrm{B}_m = \frac{1}{2nA_c} \int_0^{\frac{T_0}{2}} v_L dt \tag{2.46}$$

where n is the turn number of the windings of the inductor, A_c is the effective cross-sectional area of the magnetic core and v_L is the voltage across the filter inductor. Neglecting the winding loss, v_L is also represented by the inductive electromotive force [91], which is shown as

$$v_L \approx nA_c \frac{dB(t)}{dt} \tag{2.47}$$

And thus, the classical eddy current loss P_{eddy} can be rewritten as

$$P_{eddy} = V \frac{K_{cl} f_0}{(nA_c)^2} \int_0^{T_0} {v_L}^2 \tag{2.48}$$

Meanwhile, when the switching frequency is much higher than the grid frequency, the filter inductor voltage can be represented as the inductor voltage in every switching period which is described by the averaged switch model

$$v_{L\_i} \approx \overline{v_{L\_i}} = \overline{v_{dc}} q(t) - \overline{v_{g\_i}} = V_{dc} q(t) - \overline{v_{g\_i}} \tag{2.49}$$

where $q(t)$ is the switching function depicted in (2.21), and $\overline{v_{g\_i}}$ and $\overline{v_{dc}}$ are averaged values of the grid voltage and the dc-link voltage in the i-th switching cycle, respectively. Due to the constant dc-link voltage control, V_{dc} can be substituted for $\overline{v_{dc}}$.

Hence, (2.45) can be rewritten as

$$P_{core} = V\left(\frac{K_h f_0}{nA_c}\left(\left(\sum_{i=1}^{M} \int_{(i-1)T_s}^{iT_s} v_{L\_i} dt\right) + \int_{MT_s}^{\frac{T_0}{2}} v_{L\_(M+1)} dt\right)^x + \frac{K_{cl} f_0}{(nA_c)^2} \sum_{i=1}^{N} \int_{(i-1)T_s}^{iT_s} {v_{L\_i}}^2 dt\right) \tag{2.50}$$

where M is an integer less than or equal to $\frac{N}{2}$ and N is the total number of the switching cycles over a grid period.

In this research, a silicon steel lamination with the thickness of 0.35 mm is used as the iron core of the filter inductor due to the low cost. All design parameter of the proposed filter inductor are summarized in Table 2.3, where K_h, x and K_{cl} are obtained by nonlinear regression analysis stated in [91].

Table 2.3 Parameters for iron loss calculation

Parameters	V (kg)	n (turns)	A_c (m^2)	R_{cu} (Ω)
Value	8	40	0.003	0.07
Coefficients	K_h	x	K_{cl}	
Value	0.022871	1.685945	0.000004	

Therefore, the total power loss P_L of the filter inductor is found by adding (2.43) and (2.50)

$$P_L = P_{cu} + P_{iron} \tag{2.51}$$

2.4 Loss Distribution under Various Switching Strategies

For predicting the efficiency performance of VSIs based on the expected losses discussed above, an M-language program is built to simulate the operation of the inverter, and then estimate the power losses by iterating loss calculation over switching cycles in Matlab.

Furthermore, a prototype 10 kW single-phase grid-connected VSI with the same parameters as those listed in Table 2.2 has been implemented to demonstrate the loss model and, further, the research outcomes in this dissertation.

2.4.1 Efficiency Definitions

Efficiency is a good measure of success of a given inverter in renewable energy generation applications. High efficiency inverters are necessary not only to obtain high return on investment but also to achieve high system reliability and long lifetime operation. For grid-connected inverters, the efficiency is defined as

$$\eta_{inv} = \frac{P_{grid}}{P_{in}} \times 100\% \tag{2.52}$$

where P_{in} and P_{grid} represent the input and output power of inverters, respectively.

According to the component-level loss analysis in Section 2.3, the efficiency of the proposed VSI can be evaluated by

$$\eta_{VSI} = \frac{P_{in} - P_{cap} - P_{IGBT} - P_{Diode} - P_L}{P_{in}} \times 100\% \tag{2.53}$$

where P_{cap}, P_{IGBT}, P_{Diode} and P_L are found from (2.32), (2.41), (2.42) and (2.51), respectively.

In addition, the total efficiency taking into account all apparatus presented within the proposed generation system (shown in Fig. 2.1) is defined by the multiplication of efficiencies of both front-end PECs (η_{PEC}) and VSIs (η_{VST}).

$$\eta_{total} = \eta_{PEC} \cdot \eta_{VSI} \tag{2.54}$$

By nature of renewable energy, the efficiency of VSIs is strongly linked with the operating power level. Thus, weighted efficiency concepts with factors directly related to different power levels are proposed to evaluate the energy conversion efficiency of a given grid-connected generation system. In a solar system, a typical example is the so-called "European efficiency" [93] which is an average efficiency over a yearly power distribution corresponding to middle-Europe climate with low radiation, while for climates of higher insolation, such as the southeast of the U.S., the California Energy Commission (CEC) efficiency is defined [94]. Therefore, when η_{PEC} is assumed to be a constant, the European efficiency and the CEC efficiency can be given by (2.55) and (2.56), respectively.

$$\eta_{Euro} = \eta_{PEC} \cdot (0.03\eta_{VSI\_5\%} + 0.06\eta_{VSI\_10\%} + 0.13\eta_{VSI\_20\%} + 0.10\eta_{VSI\_30\%} + 0.48\eta_{VSI\_50\%} + 0.20\eta_{VSI\_100\%}) \tag{2.55}$$

$$\eta_{CEC} = \eta_{PEC} \cdot (0.04\eta_{VSI\_10\%} + 0.05\eta_{VSI\_20\%} + 0.12\eta_{VSI\_30\%} + 0.21\eta_{VSI\_50\%} + 0.53\eta_{VSI\_75\%} + 0.05\eta_{VSI\_100\%}) \tag{2.56}$$

where $\eta_{VSI\_x\%}$ is the efficiency of the VSI at the x percent of the rated power.

Hence, in order to compare the efficiency performance of various VSIs for PV generation, η_{Euro_VSI} and η_{CEC_VSI} are used in this dissertation and defined as

$$\eta_{Euro\_VSI} = \frac{\eta_{Euro}}{\eta_{PEC}} \tag{2.57}$$

$$\eta_{CEC\_VSI} = \frac{\eta_{CEC}}{\eta_{PEC}} \tag{2.58}$$

2.4.2 Efficiency Model with Unipolar SPWM

As discussed in Section 2.3, the loss distribution of the VSI is dependent on switching strategies. High frequency unipolar SPWM is one of the most widely used techniques for dc to ac inverters with the advantages of low switching losses and high dc voltage utilization [95]-[97]. Fig. 2.12 shows the switching waveforms of the VSI with a typical unipolar SPWM strategy. In a unipolar SPWM method, the amplitude of the inverter output voltage (v_{ab}) is determined by comparing a sinusoidal reference wave V_{ref}, with a triangular carrier signal of amplitude V_c, known as modulation index M, which is defined as

$$M = \frac{V_{ref}}{V_c} \tag{2.59}$$

Based on the inverter equivalent circuit shown in Fig. 2.8, when the unit power factor is applied, (2.59) can be rewritten by

$$M = \frac{\sqrt{2{V_g}^2 + 2(X_L I_{ref})^2}}{V_{dc}} \qquad (M \in [0, 1]) \tag{2.60}$$

where V_g is the RMS value of the grid voltage, I_{ref} is the RMS value of the reference grid current, and X_L is the impedance of the filter inductor. Neglecting the resistance of the inductor, X_L is given by

$$X_L = \omega_0 L \tag{2.61}$$

where ω_0 is the grid angular frequency and L is the inductance of the filter inductor.

As the switching frequency is much higher than the grid frequency, the duty cycle under unipolar SPWM control can be given by

$$d(i) = Msin\left(iT_s\omega_0 - \frac{T_s}{2}\omega_0\right) \qquad (i = 1, 2, 3, \dots, N) \tag{2.62}$$

where T_s represents the switching period, i refers to the i-th switching period and N is the integer number of $\frac{T_0}{T_s}$; T_0 represents the grid period.

Thus, the values of the effective duty cycle for every IGBT and diode in each switching period can be expressed as

$$\begin{cases} d_{IGBT1\_i} = 1 \\ d_{IGBT4\_i} = d(i) \\ d_{D3\_i} = 1 - d(i) \\ others = 0 \end{cases} \quad (in\ the\ positive\ of\ T_0)$$

$$\begin{cases} d_{IGBT2\_i} = 1 \\ d_{IGBT3\_i} = |d(i)| \\ d_{D4\_i} = 1 - |d(i)| \\ others = 0 \end{cases} \quad (in\ the\ nagative\ of\ T_0) \tag{2.63}$$

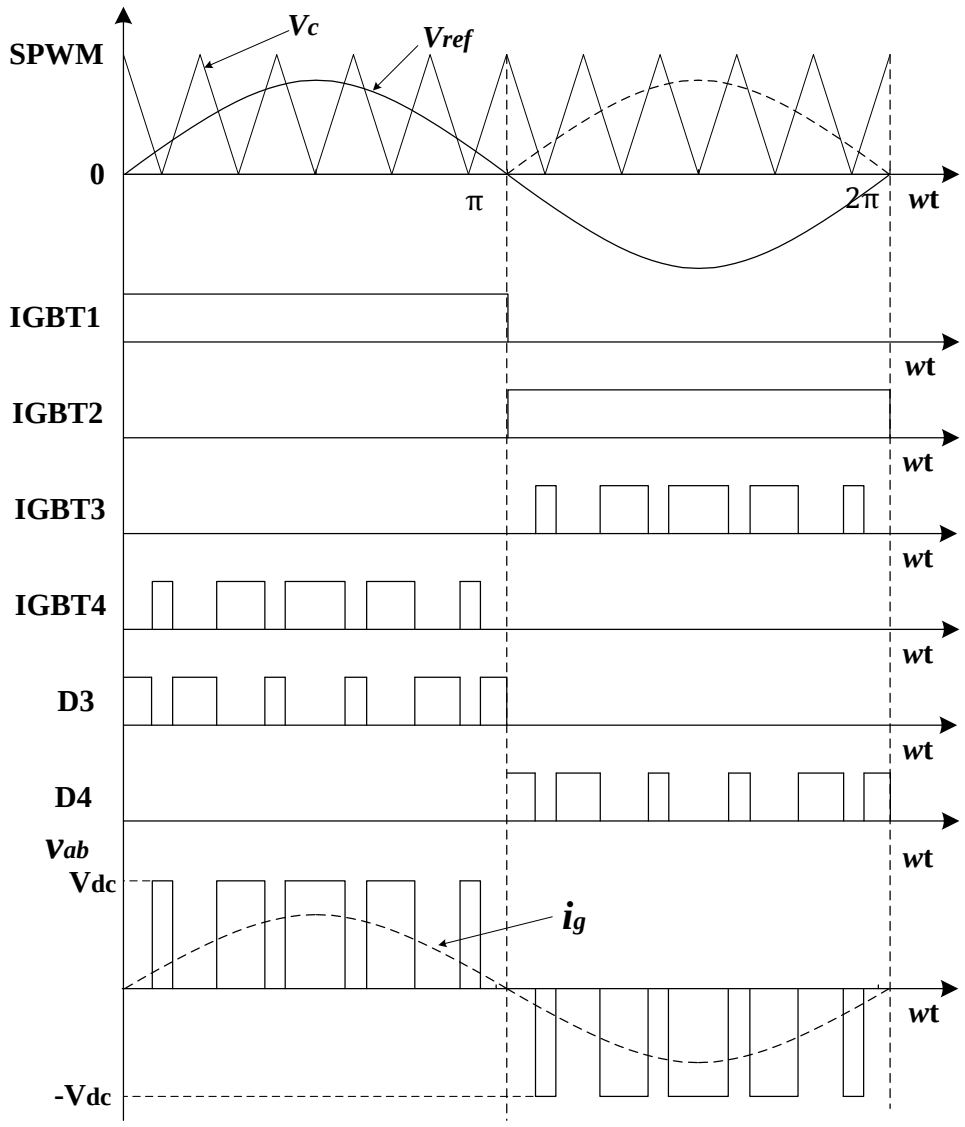


Fig. 2.12 Switching waveforms of the VSI with unipolar SPWM

An M-language program is used to estimate the power loss distribution of the VSI with different modulation techniques, and is found in Appendix A. Fig. 2.13 shows the power loss distribution of the VSI with unipolar SPWM control which is obtain by substituting (2.63) into (2.32), (2.41), (2.42) and (2.51). The VSI operates at the rated power of 10

kW with a 20 kHz switching frequency; the junction temperature of IGBTs is assumed to be 60 ℃ when the ambient temperature is 20 ℃ with the proper cooling system.

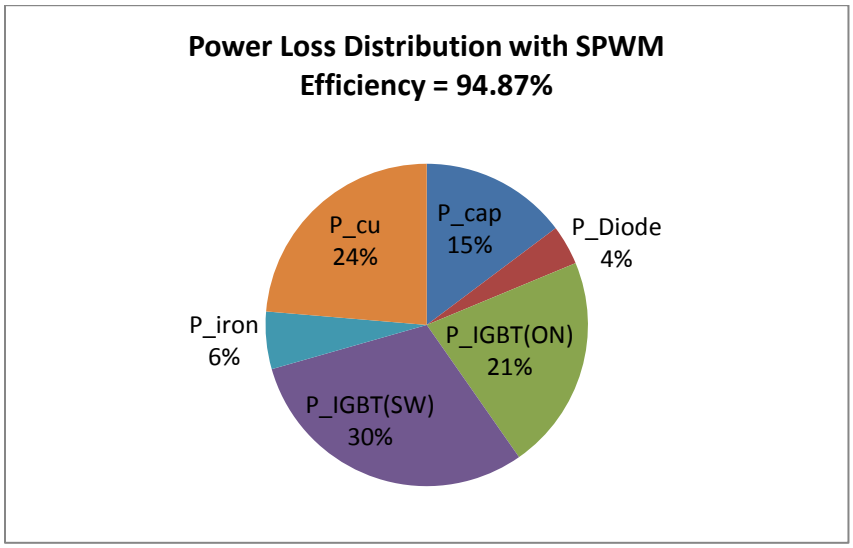


Fig. 2.13 Power loss distribution with SPWM under rated power

Fig. 2.14 shows the efficiency of the 10 kW VSI prototype inverter estimated using the loss model and measured through tests. The experimental results demonstrate the validity of the proposed loss analysis model. The errors between the simulation and actual measurement are derived from the power losses of digital control circuits, power conductors, fuses, contactors and other VSI components.

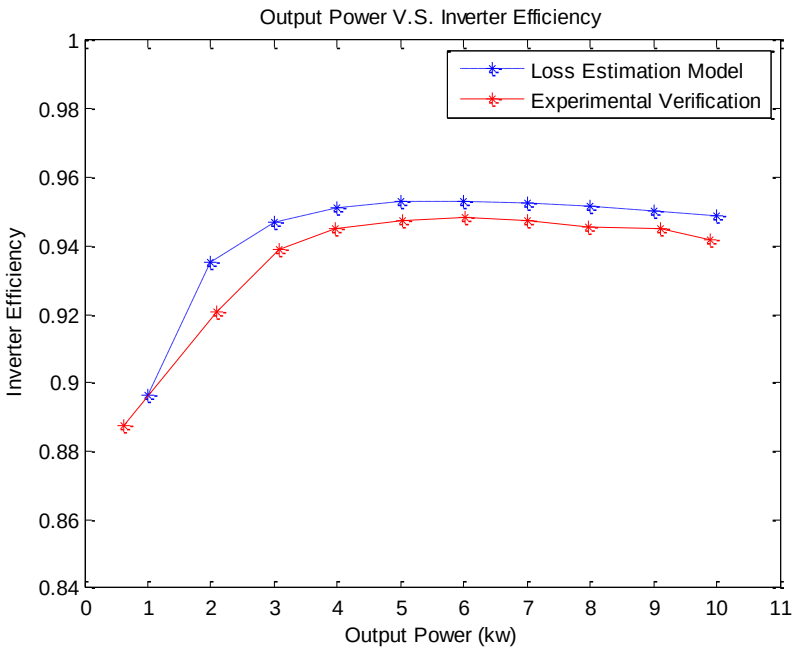


Fig. 2.14 Efficiency of VSIs with SPWM

2.4.3 Efficiency Model with CCPWM

In grid-connected generation systems, the quality of output current fed to the grid is a main concern. Hence, CCPWM strategies are often implemented for VSIs due to their better current performance with fast and accurate current tracking. Following the analysis of the averaged switch model in Section 2.3.1, the average inductor voltage of the VSI can be expressed as

$$L\frac{d\overline{i_g}}{dt} = V_{dc}d - \overline{v_g} \tag{2.64}$$

According to the definition of the derivative of $\overline{i_g}$, (2.64) can be rewritten as

$$L\frac{i_g(t+T_s)-i_g(t)}{T_s} = V_{dc}d - \overline{v_g} \tag{2.65}$$

And thus, when the unit power factor is applied and current ripples are neglected, the duty cycle of each switching period with CCPWM can be obtain by

$$d(i) = \frac{\sqrt{2}I_{ref}L}{V_{dc}T_s}\left(sin(iT_s\omega_0) - sin(iT_s\omega_0 - T_s\omega_0)\right) + \frac{\sqrt{2}V_g}{V_{dc}} sin\left(iT_s\omega_0 - \frac{T_s}{2}\omega_0\right) \quad (i = 1,2,\cdots,N) \tag{2.66}$$

where $\sqrt{2}V_g sin\left(iT_s\omega_0 - \frac{T_s}{2}\omega_0\right)$ represents the averaged grid voltage in the i-th switching cycle.

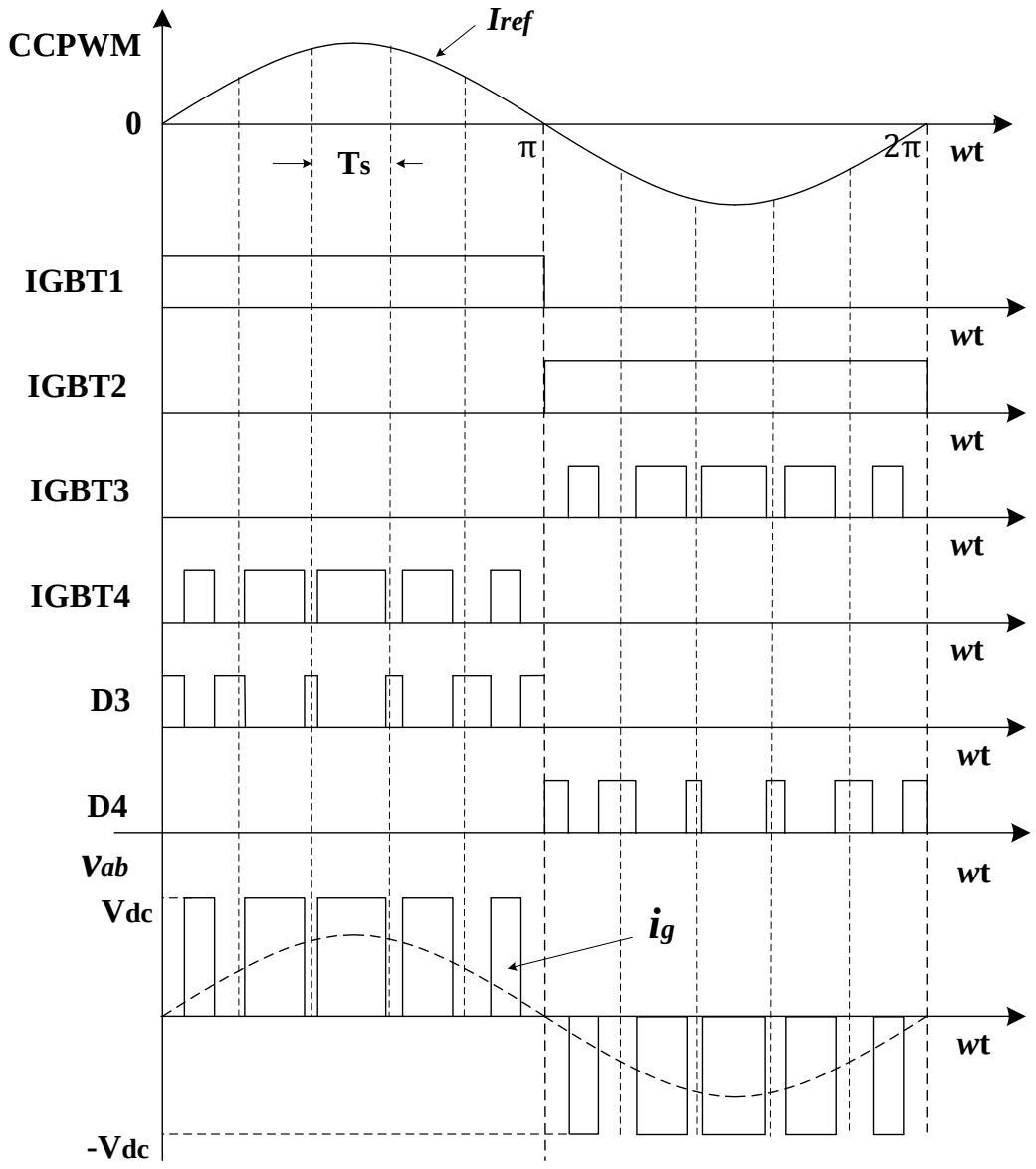


Fig. 2.15 Switching waveforms of the VSI with CCPWM

CCPWM for the investigated VSI has the same switching function as SPWM which is given in (2.63). Substituting (2.66) into (2.63), the loss distribution and efficiency characteristics of the VSI are obtained and shown in Fig. 2.16 and Fig. 2.17, respectively. Due to the similar modulation method, the theoretical maximum efficiency under

CCPWM control (the dashed line in Fig. 2.17) is approximately equal to that with a unipolar SPWM strategy in ideal condition that means the errors from the digital control circuit, such as delays, sensor deviations and etc., are neglected. However, the experimental efficiency with CCPWM (the solid line in Fig. 2.17) is a little bit higher than that with SPWM (the solid line in Fig. 2.14) as a result of better current harmonic performance when the current control algorithm is carried out.

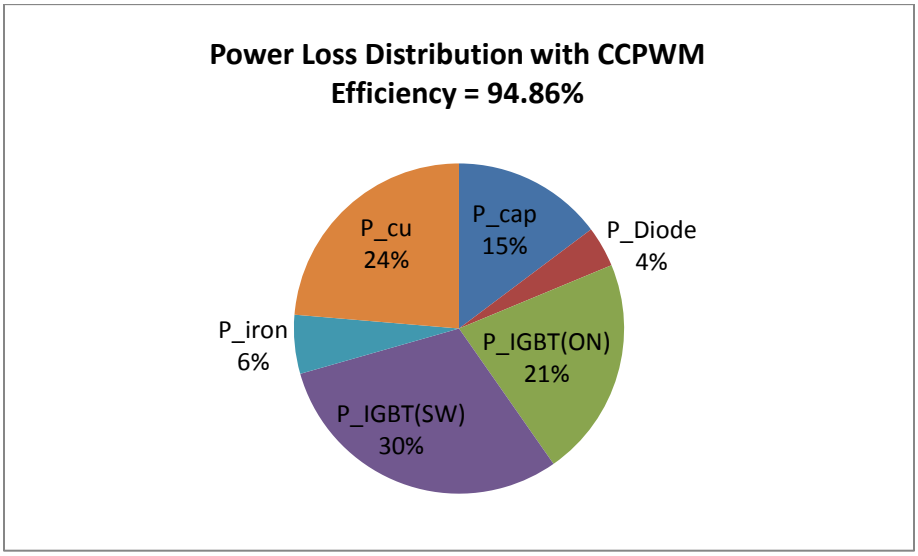


Fig. 2.16 Power loss distribution with CCPWM at rated power

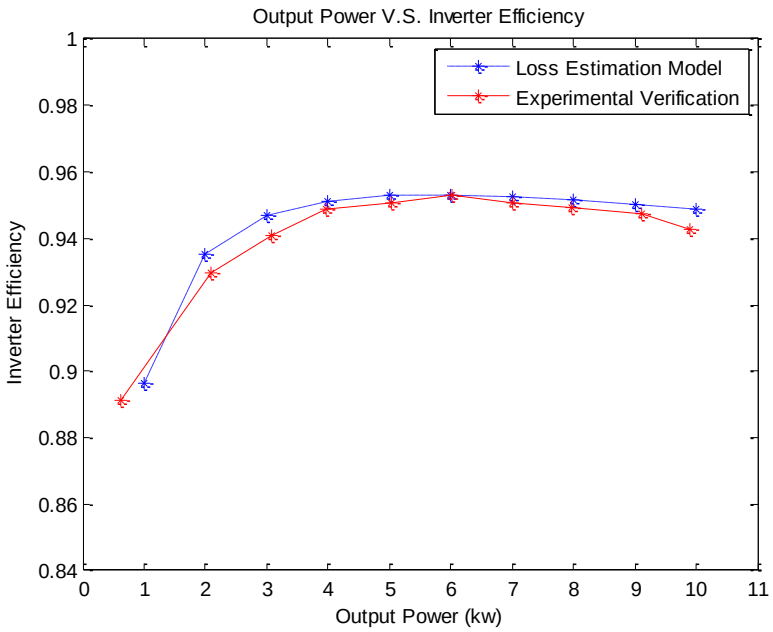


Fig. 2.17 Efficiency of VSIs with CCPWM

2.4.4 Efficiency Model with Improved CCSVPWM

CCSVPWM is another typical approach for grid-connected VSIs to achieve good quality of the power fed to the grid. Compared with the traditional CCPWM strategy, CCSVPWM control has the similar current control algorithm, but better performance of high dc voltage utilization, fast dynamic response and easy digital implementation [98], [99] as a result of implementation of SVPWM technique. Based on that, an improved CCSVPWM control scheme is introduced in this dissertation to reduce output current harmonics through doubling the frequency of the current ripple [96], [100].

As shown in Fig. 2.1, there are four IGBTs in the full-bridge inverter, which can be in either state of ON or OFF, meaning of 1 or 0. As the driving signals for the switches of

the same arm are complimentary, the switch states of the upper arm IGBTs, which is represented by S_1 and S_3, can be used to determine the output voltage of the inverter, and thus, the combination of these four switches can produce four possible voltage space vectors to describe the operation of the proposed VSI. Table 2.4 summarizes voltage space vectors along with the corresponding operation model and output voltage from the inverter. Accordingly, the output voltage in a space vector form is given in Fig. 2.18, where $V_2(1,1)$, $V_4(0,0)$are zero vectors and $V_1(1,0)$, $V_3(0,1)$ are active vectors whose values are $+V_{dc}$ and $-V_{dc}$, respectively.

Table 2.4 Voltage space vectors for operation of the VSI

Voltage Space Vector	Operation Mode	Switching States		Output Voltage
		S_1	S_3	v_{ab}
V_1	1	1	0	$+V_{dc}$
V_2	2	1	1	0
V_3	3	0	1	$-V_{dc}$
V_4	4	0	0	0

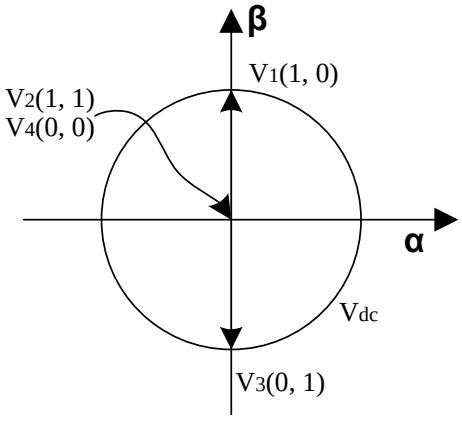


Fig. 2.18 Voltage space vectors of the VSI

In traditional CCSVPWM, a set of an active vector and a zero vector can be selected to synthesize a desired reference voltage obtained from a current controller in each switching period. For example, vectors V_1 and V_2 work together during every switching period in the positive half cycle of the grid current in sequence, "V_2-V_1-V_2". An improved CCSVPWM has been implemented in this dissertation to achieve a better current quality through introducing and positioning the zero vectors to the switching sequence [101]. Thus, the switching waveforms of the VSI with CCSVPWM is shown in Fig. 2.19 with a sequential switching process as "V_2-V_1-V_4-V_1-V_2 ⋯ V_2-V_1-V_4-V_1-V_2 ⋯" in the positive half cycle and "V_4-V_3-V_2-V_3-V_4 ⋯ V_4-V_3-V_2-V_3-V_4 ⋯" in the negative half cycle. It is clear that the frequency of the output current ripple is doubled by splitting the pulse width in a switching period. As a result, the magnitude of ripple current is reduced to a half with the same switching frequency.

Assuming that the ideal current controller is implemented, the conduction time of active vectors in each switching period can be calculated as

$$T_{on} = \frac{L\frac{i_g(t+T_s)-i_g(t)}{T_s}+\overline{v_g}}{V_{dc}} \cdot T_s \tag{2.67}$$

From (2.67), it is noticed that if $\frac{T_{on}}{T_s}$ is seen as a duty cycle, every $\frac{T_{on}}{T_s}$ during a switching period has the same expression as (2.66). However, due to more zero vectors added, the values of the effective duty cycle for every IGBT and diode in each switching period are different from those in either SPWM control or CCPWM control, and can be given by

$$\begin{cases} d_{IGBT1\_i} = d_{IGBT4\_i} = 0.5 + 0.5d(i) \\ d_{D2\_i} = d_{D3\_i} = 0.5 - 0.5d(i) \qquad (in\ the\ positive\ of\ T_0) \\ others = 0 \end{cases}$$
$$\begin{cases} d_{IGBT2\_i} = d_{IGBT3\_i} = 0.5 + 0.5|d(i)| \\ d_{D1\_i} = d_{D4\_i} = 0.5 - 0.5|d(i)| \qquad (in\ the\ nagative\ of\ T_0) \\ others = 0 \end{cases} \tag{2.68}$$

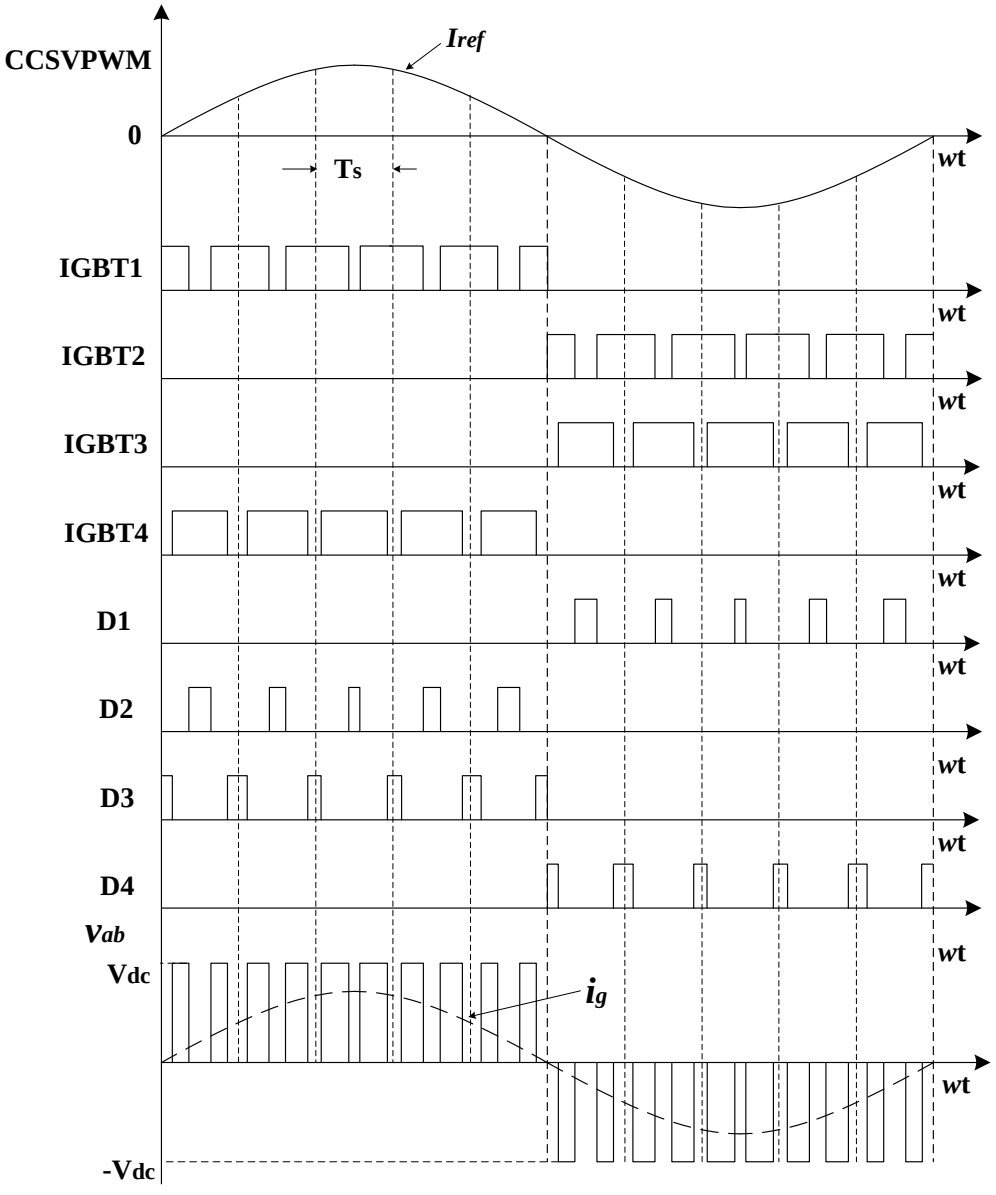


Fig. 2.19 Switching waveforms of the VSI with improved CCSVPWM

Correspondingly, the power loss distribution and efficiency curves of the VSI under the improved CCSVPWM strategy are shown Fig. 2.20 and Fig. 2.21, respectively. Obviously, the maximum inverter efficiency is 93.31%, which is lower than that with unipolar SPWM or CCPWM, because in CCSVPWM control, there are two IGBTs switching on/off during each half cycle of the grid period, resulting in twice the switching losses.

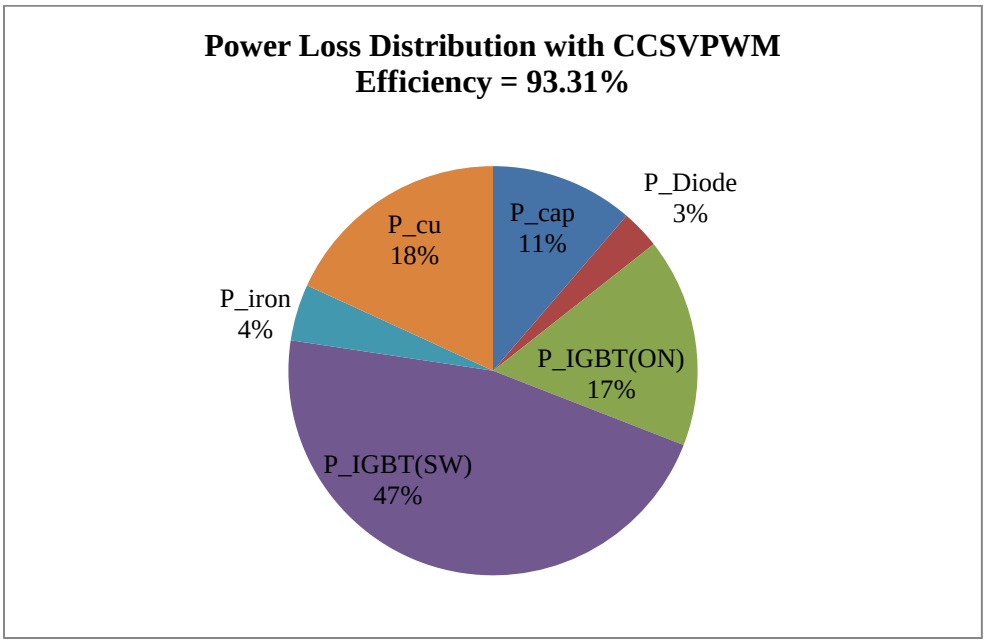


Fig. 2.20 Power loss distribution with CCSVPWM at rated power

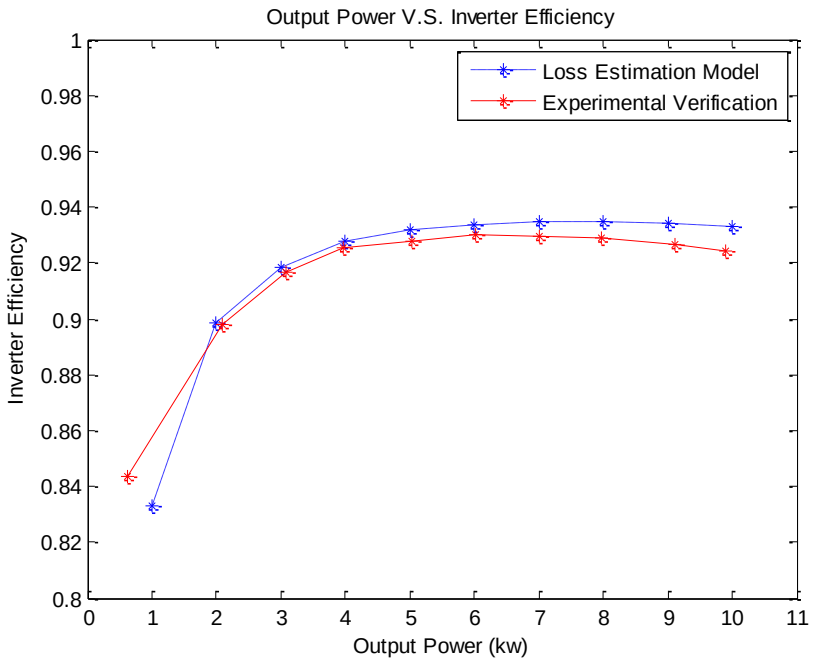
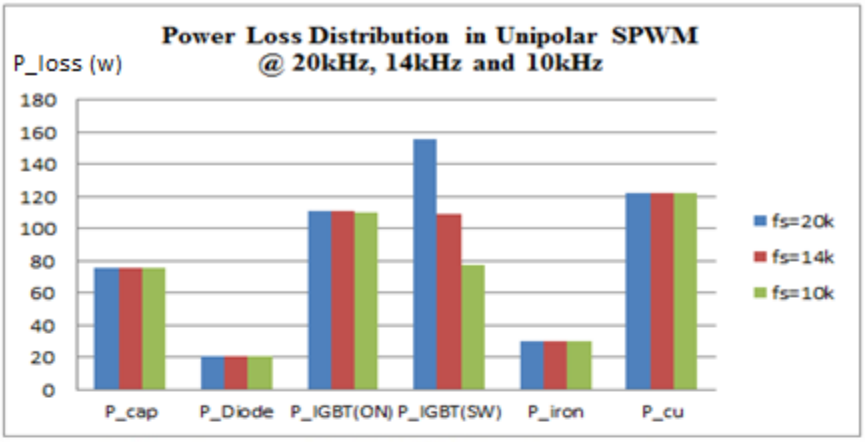


Fig. 2.21 Efficiency of VSIs with CCSVPWM

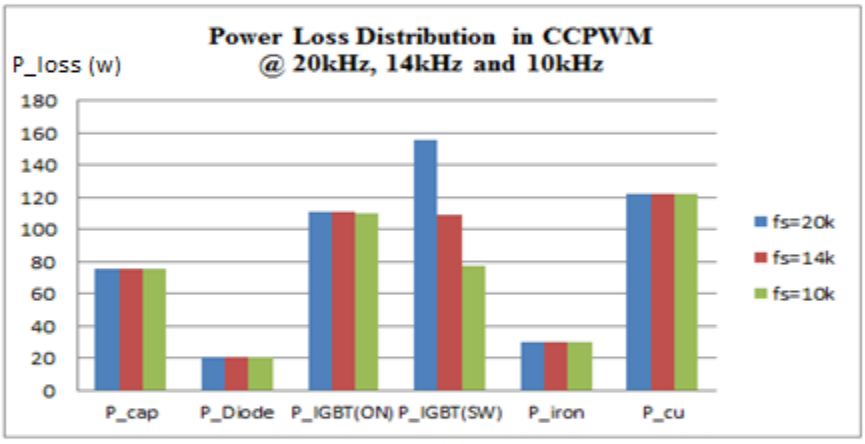
2.4.5 Key Factors in Contributions to Power Dissipation

In Section 2.4, the estimation model of power loss distribution has been demonstrated to be effective in predicting the efficiency of the proposed VSI with a given modulation strategy. Using this loss estimation model, Fig. 2.22 illustrates variations of power consumption of the investigated VSI system at the rated power with various switching frequencies based on the control techniques of unipolar SPWM, CCPWM and CCSVPWM, respectively. It is observed that capacitor losses, conduction losses of IGBTs and diodes, and the losses of the filter inductor are independent of the switching frequency and modulation techniques whereas the switching losses are almost proportional to the switching frequency and influenced a lot by the control strategies used.

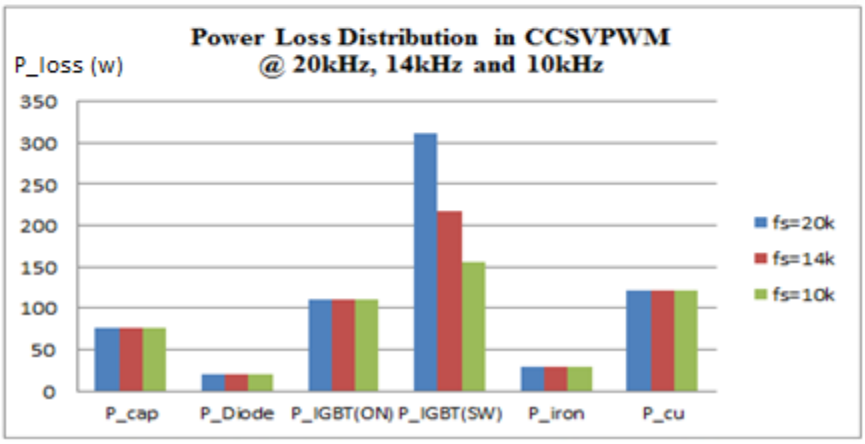
Therefore, reducing the switching frequency is one of the most effective ways to improve the efficiency of single-phase grid-connected VSIs.



(a)



(b)



(c)

Fig. 2.22 Power loss distribution at variable switching frequencies in (a) Unipolar SPWM (b) CCPWM (c) CCSVPWM

In addition, the voltage of the dc-link is another important factor in determining the total losses consumed in the VSI which is stabilized at a preset reference value by the constant dc-link voltage control. As depicted in Fig. 2.23, it is clear that as the dc-link voltage increases, the efficiency of the VSI deceases. However, in order to prevent over-modulation phenomena, the minimum dc-link voltage is restricted by the maximum value of the grid voltage to a linear controllable region [102] that makes sure that either the modulation index of SPWM control or the absolute value of the duty cycle during each switching period for current control algorithms is less than or equal to one. As the maximum acceptable RMS value of the grid voltage is 264 V stated by international standards, considering possible voltage fluctuation caused by dc-link capacitors, a reasonable value of 390 V is set as the reference magnitude of the dc-link voltage to achieve a better efficiency performance of the VSI.

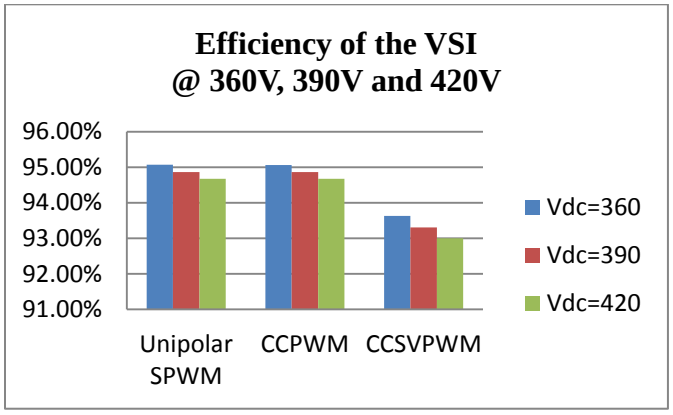


Fig. 2.23 Power loss distribution with different dc-link voltages

2.5 Summary

In Chapter 2, the schematic of the VSI under investigation is presented, which is primarily composed of the dc-link and full-bridge inverter. The constant voltage control for the dc-link is developed to decouple and balance the power between the output of front-end PECs and the input of the full-bridge inverter. Also, the operation of the full-bridge inverter is detailed in this chapter and modeled by an averaged switch method.

In addition, the loss analysis of each part of the VSI has been discussed, including dc-link capacitor losses, on-state losses and switching losses of semiconductor devices and the filter losses. When the switching frequency of the inverter is much higher than the grid frequency, losses of the VSI under a given operation condition can be estimated by a M-language program in Matlab based on the averaged switch model and verified by experiments conducted on a 10 kW single-phase grid-connected inverter prototype.

Finally, by comparing the efficiencies of the VSI with three typical modulation techniques at variable switching frequencies, it becomes evident that the switching losses are the major controllable losses of the VSI as determined by the switching frequency and control strategies used. Therefore, choosing an optimal switching frequency is considered as one of the most effective ways to improve the VSI efficiency.

3 Current Harmonic Estimation for Single-Phase Grid-Connected Inverters

3.1 Introduction

Harmonic distortion of grid current is the key parameter to gauge the performance of power quality for grid-connected inverter output and depends on many factors such as control algorithms, modulation techniques, switching frequencies of power electronics devices and so on. In this Ph.D. research, one of the most important goals is to identify the critical factors that influence the grid current harmonic distortion. A novel method to calculate the total current harmonic contents is presented firstly in this chapter through estimating the RMS value of output current ripples. However, as current harmonics in high frequency ranges are normally attenuated or even eliminated by filter technologies, only the low-order current harmonic distortion is of primary concern for the grid power quality and required by grid interconnection standards. Accordingly, two evaluation models of THD and TDD of the grid current based on the requirement of grid interconnection standards are built through deducting the high frequency harmonic component from the total harmonic content. Both models are verified by experiments conducted on a 10 kW single-phase inverter with the improved CCSVPWM strategy.

3.2 THD/ TDD Model Based on Output Current Ripples

As discussed in Chapter 2, the current fed to the grid inevitably has some harmonic content even regulated from a well-designed VSI — the current varies when the

conducting state of the inverter changes in every switching period. A typical output grid current waveform is depicted in Fig. 3.1(a). Under steady-state conditions, this grid current is a periodic function of time T_0 and can be represented by a Fourier series described in [31]. Fourier analysis is a standard method to identify the harmonic contents for a PWM control, but it is not an effective and efficient way when a high or a non-integer carrier-to-fundamental ratio is applied [103]. In those cases, the interharmonics [104] would have to be considered and performed by Fourier analysis, making the analysis by a conventional Fourier series quite difficult.

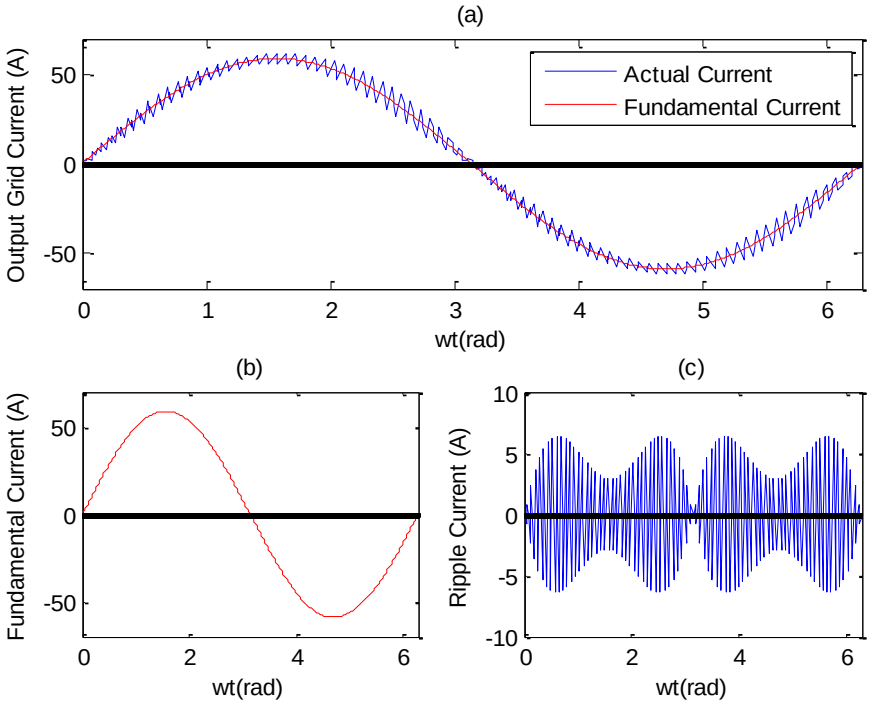


Fig. 3.1 Grid current and harmonics (a) output grid current (b) fundamental component of output grid current (c) current ripples of output grid current

Double Fourier series approach presented in [105] provides a solution of this problem by reformulating the grid current as a periodic two-dimensional function of two independent time variables corresponding to the fundamental frequency and the switching frequency respectively. Consequently, the function of the grid current can be decomposed by using a double Fourier series and performs the harmonic analysis involving contributions from both frequencies. The grid current represented by a double Fourier series is given in the form of

$$i_g(t) = \frac{a_{00}}{2} + \sum_{n=1}^{+\infty}(a_{0n}\cos n\omega_0 t + b_{0n}\sin n\omega_0 t) + \sum_{m=1}^{+\infty}(a_{m0}\cos m\omega_s t + b_{m0}\sin m\omega_s t) + \sum_{m=1}^{+\infty}\sum_{n=\pm 1}^{\pm\infty}[a_{mn}\cos(n\omega_0 t + m\omega_s t) + b_{mn}\sin(n\omega_0 t + m\omega_s t)] \quad (3.1)$$

where ω_0 and ω_s are the angular frequencies of the grid and switching behaviors, respectively. $\frac{a_{00}}{2}$ is the dc component of the output current and the coefficients are defined as follows:

$$\begin{cases} a_{0n} = \frac{1}{\pi}\int_0^{2\pi} i_g(\omega_0 t, \omega_s t)\cos n\omega_0 t\, d\omega_0 t \\ b_{0n} = \frac{1}{\pi}\int_0^{2\pi} i_g(\omega_0 t, \omega_s t)\sin n\omega_0 t\, d\omega_0 t \end{cases} \quad (3.2a)$$

$$\begin{cases} a_{m0} = \frac{1}{\pi}\int_0^{2\pi} i_g(\omega_0 t, \omega_s t)\cos m\omega_s t\, d\omega_s t \\ b_{mo} = \frac{1}{\pi}\int_0^{2\pi} i_g(\omega_0 t, \omega_s t)\sin m\omega_s t\, d\omega_s t \end{cases} \quad (3.2b)$$

$$\begin{cases} a_{mn} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} i_g(\omega_0 t, \omega_s t)\cos(n\omega_0 t + m\omega_s t)\, d\omega_s t d\omega_0 t \\ b_{mn} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} i_g(\omega_0 t, \omega_s t)\sin(n\omega_0 t + m\omega_s t)\, d\omega_s t d\omega_0 t \end{cases} \quad (3.2c)$$

From (3.1), the expression of the grid current by the double Fourier series typically contains four terms. The first term is the dc component. The second term defines the fundamental component and baseband harmonics. The third term corresponds to the

frequency of switching behaviors and its harmonics, which can be neglected when EMI effect is excluded. And the final term summarizes all interharmonic components. When a proper control algorithm is applied for VSIs, the dc term of the grid current becomes zero (i.e., $a_{00} = 0$) and then (3.1) can be rewritten as

$$i_g(t) = \sqrt{2}I_1 \sin(\omega_0 t + \varphi_1) + \sum_{n=2}^{+\infty}(a_{0n} \cos n\omega_0 t + b_{0n} \sin n\omega_0 t) + \sum_{m=1}^{+\infty} \sum_{n=\pm 1}^{\pm \infty}[a_{mn} \cos(n\omega_0 t + m\omega_s t) + b_{mn} \sin(n\omega_0 t + m\omega_s t)] \quad (3.3)$$

where I_1 is the RMS value of the fundamental component of the grid current and φ_1 is the output power factor angle which is obtained from

$$\varphi_1 = \tan^{-1} \frac{a_{01}}{b_{01}} \quad (3.4)$$

From (3.3), it is clear that the actual grid current can be represented by a fundamental component plus a series of harmonic terms. Meanwhile, the waveform of the grid current can be also seen as a superposition of a sinusoidal wave (Fig. 3.1(b)) and non-sinusoidal waves (Fig. 3.1(c)). The sine wave is the fundamental current whose magnitude is almost equal the reference current value in control, while the non-sinusoidal waves are the current ripples which are caused by switching behaviors of the inverter [66], [106]. Thus, the current ripples show in the Fig 3.1(c) can be used to represent the harmonics part of the output grid current, as

$$\Delta i_g(t) = \sum_{n=2}^{+\infty}(a_{0n} \cos n\omega_0 t + b_{0n} \sin n\omega_0 t) + \sum_{m=1}^{+\infty} \sum_{n=\pm 1}^{\pm \infty}[a_{mn} \cos(n\omega_0 t + m\omega_s t) + b_{mn} \sin(n\omega_0 t + m\omega_s t)] \quad (3.5)$$

where Δi_g refers to the current ripples of the output grid current.

By definition in [31], the relationship between current THD, TDD and current ripples can be obtained as

$$\begin{cases} THD = \frac{\sqrt{{I_g}^2 - {I_1}^2}}{I_1} = \frac{\Delta I_{g\_RMS}}{I_1} & (3.6a) \\ TDD = \frac{\sqrt{{I_g}^2 - {I_1}^2}}{I_m} = \frac{\Delta I_{g\_RMS}}{I_m} & (3.6b) \end{cases} \tag{3.6}$$

where ΔI_{g_RMS} is the RMS value of Δi_g and I_m is defined as the "maximum load current integrated demand (15 or 30 minutes)" stated in [107].

Therefore, it is of interest to calculate the RMS value of the current ripples in this dissertation in order to estimate the THD or TDD of the grid current. Fig. 3.2 illustrates the relationship between the actual grid current and current ripples. When the switching frequency of the inverter is much higher than the grid frequency, the slope of the fundamental current over a switching period can be seen as a constant. Hence, if the current at the middle point of each switching cycle is selected as the reference current, the initial point and the final point of the actual current in each switching period are proven to be on the curve of the fundamental current when both a proper current control algorithm and a unit power factor are applied (see the proof in Appendix B). As a result, a waveform of the ripple current is presented in Fig. 3.2(b) by removing the fundamental component from the actual grid current. It is observed that the ripple current Δi_g is represented by a periodic triangular waveform, which has the same frequency as the switching frequency of the inverter. With symmetric PWM control, the triangular waveform of Δi_g in each cycle of T_s is supposed to be symmetric with respect to the

central point (point B in Fig. 3.2), and the ripple current at the start point (point A in Fig. 3.2), midpoint and the end point (point D in Fig. 3.2) are all equal to zero.

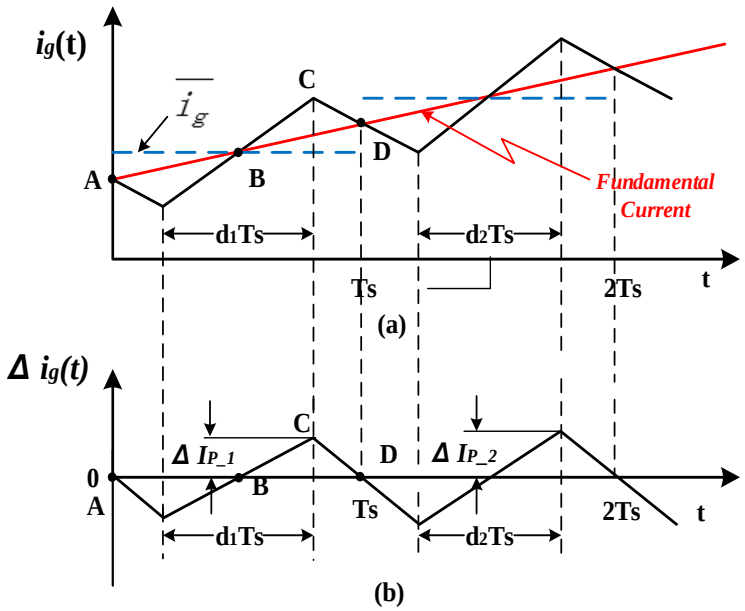


Fig. 3.2 Waveforms of actual grid current and current ripples (a) output grid current (b) current ripples

Therefore, the RMS value of Δi_g during each switching period can be obtained by its individual peak value of the current ripple as

$$\Delta I_{g\_RMS\_i} = \Delta I_{p\_i}\sqrt{\frac{1}{3}} \tag{3.7}$$

where $\Delta I_{g\_RMS\_i}$ and ΔI_{p_i} are the RMS and peak values of Δi_g in the i-th switching cycle, respectively. ΔI_{p_i} is determined by a given control algorithm and its corresponding switching frequency.

Accordingly, the overall RMS value of the waveform of current ripples over a complete grid cycle can be approximated satisfactorily by combing the individual RMS values of each switching cycle given from (3.7), which is calculated by

$$\Delta I_{g\_RMS} = \sqrt{\frac{2}{N}\sum_{i=1}^{N/2} \Delta I_{g\_RMS\_i}{}^2} \tag{3.8}$$

where N is the integer number of the switching cycles over a grid period.

3.3 THD/ TDD Estimation Model

3.3.1 RMS Value of Current Ripples under CCSVPWM Control

According to the analysis in Chapter 2, an improved CCSVPWM strategy is proposed in this Ph.D. research with the advantages of low harmonic current output and easy implementation for a DSP-based control system. The typical waveforms of the output grid current and corresponding current ripples based on the CCSVPWM control are sketched in Fig. 3.3. In the positive half cycle of the grid period, operations of the inverter are alternated between Mode 1 and Mode 2 in each switch period. During the subinterval in Mode 1, output current flowing though the filter inductor will increase with a slope of $(v_{dc} - v_g)/L$. Next, with operation in Mode 2, the current will change with a slope of $-v_g/L$. This process repeats during the second and succeeding half switching periods when the CCSVPWM strategy is implemented. As a result, the frequency of current ripples is doubled and four small humps are made out in the waveform of the ripple current during each switching period. Compared with a traditional CCPWM control, the peak ripple current in each switching period is reduced by half and the

corresponding current THD/ TDD is half of that with CCPWM control when the same switching frequency is applied.

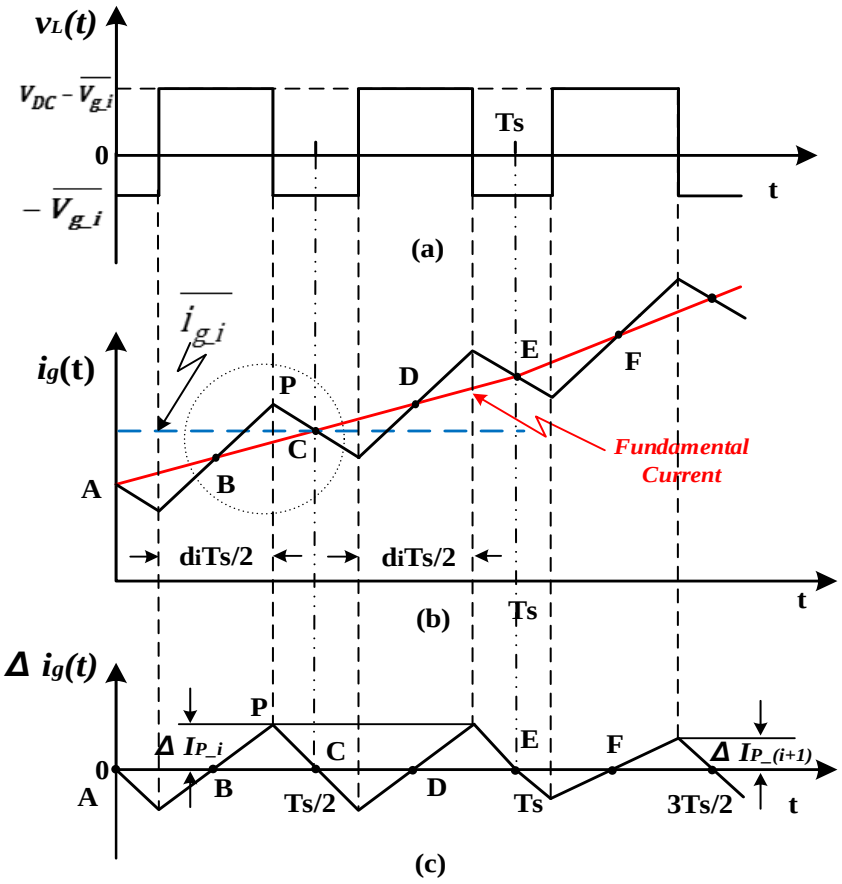


Fig. 3.3 Waveforms of actual grid current and current ripples in CCSVPWM (a) voltage across the filter inductor (b) output grid current (c) current ripples

Fig. 3.4 shows an enlarged view of the dashed portion of Fig. 3.3(b), where k_α and k_γ represent the rates of the grid current change under the operation of Mode 1 and Mode 2 respectively, which are expressed in units of amps per second, while k_β refers to the rate of change of the fundamental current. In each switching period, k_α and k_γ can be

considered to remain unchanged since both the dc-link voltage and the grid voltage are approximately constant, which can be given by

$$\begin{cases} k_\alpha = \frac{1}{L}(V_{dc} - \overline{v_{g\_i}}) \\ k_\gamma = -\frac{\overline{v_{g\_i}}}{L} \end{cases} \tag{3.9}$$

where V_{dc} represents the constant dc-link voltage and $\overline{v_{g\_i}}$ is defined as the average grid voltage over the i-th switching period. Due to the approximately linear change of the grid voltage during a switching cycle, $\overline{v_{g\_i}}$ can be expressed by the actual grid voltage at the every midpoint V_{g_x} as

$$\overline{v_{g\_i}} = V_{g\_x} = \sqrt{2}V_g \sin(iT_s\omega_0 - 0.5T_s\omega_0) \quad (i = 1, 2, 3, \cdots) \tag{3.10}$$

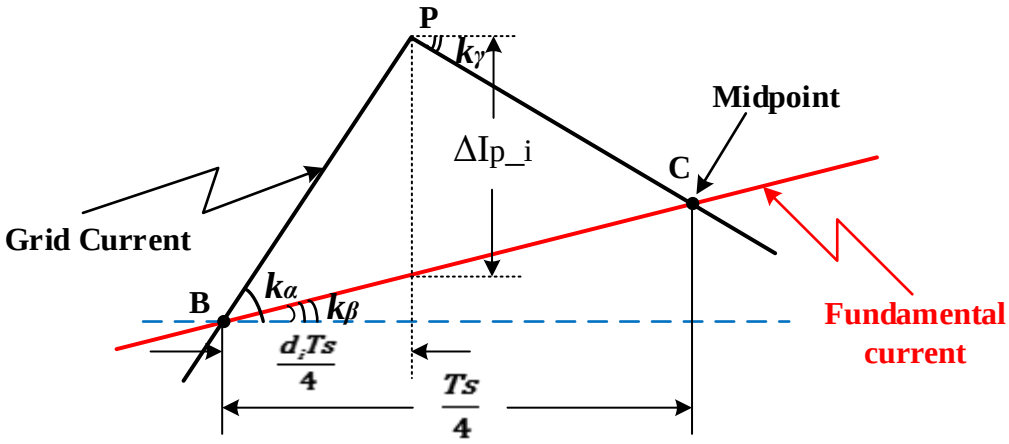


Fig. 3.4 Enlarged view of the dashed portion of Fig. 3.3(b)

Meanwhile, k_β can be seen as a constant over a switching period, when the switching frequency is much higher than the grid frequency. For example, during the switching period $t_A \rightarrow t_E$ (t_A and t_E are the time at the point A and point E) in Fig. 3.3, the currents

at both point A and point E are proved on the fundamental current curve with a proper current control, and thus k_β can be defined as

$$k_\beta = \frac{I_E - I_A}{T_s} \tag{3.11}$$

where I_A and I_E are the currents at the point A and point E.

Therefore, each of the quarter points in a switching cycle (like point A, B, C and D shown in Fig. 3.3) lay on the fundamental current curve and four humps shown on the current ripple waveform have the same peak magnitude. This maximum value of current ripples is expressed from Fig. 3.4 by

$$\Delta I_{p\_i} = (k_\alpha - k_\beta) \cdot \frac{d_i T_s}{4} \tag{3.12}$$

where d_i represents the duty cycle which is given from the corresponding current control algorithm.

Substituting (3.9), (3.10) and (3.11) into (3.12), the peak current ripple in a switching period is formulized as

$$\Delta I_{p\_i} = \left(\frac{V_{dc} - V_{g\_C}}{L} - \frac{I_E - I_A}{T_s}\right) \cdot \frac{d_i T_s}{4} \tag{3.13}$$

where V_{g_C} is the grid voltage at midpoint C of the period $t_\mathrm{A} \rightarrow t_\mathrm{E}$, equal to $\sqrt{2}V_g \sin(\omega_0 t_C)$. As discussed in Section 2.4, d_i with an ideal current controller can be given from (2.65) based on the averaged switching model as

$$d_i = \frac{1}{V_{dc}}\left(L\frac{I_E - I_A}{T_s} + V_{g\_C}\right) \tag{3.14}$$

Considering that both I_A and I_E are on the reference (fundamental) current curve, when the unit power factor is applied, $(I_E - I_A)$ can expressed as

$$\begin{aligned} I_E - I_A &= \sqrt{2} I_{ref} \sin(\omega_0 t_E) - \sqrt{2} I_{ref} \sin(\omega_0 t_A) \\ &= 2\sqrt{2} I_{ref} \cos\frac{\omega_0 t_E + \omega_0 t_A}{2} \sin\frac{\omega_0 t_E - \omega_0 t_A}{2} \\ &= 2\sqrt{2} I_{ref} \cos\frac{\omega_0 t_E + \omega_0 t_A}{2} \sin\frac{\omega_0 T_s}{2} \end{aligned} \tag{3.15}$$

where I_{ref} is the RMS value of the reference output current demanded for specific input condition.

As we know, when $\frac{\omega_0 T_s}{2} \ll 1$, $\sin\frac{\omega_0 T_s}{2}$ is approximately equal to $\frac{\omega_0 T_s}{2}$. Furthermore, $\frac{\omega_0 t_E + \omega_0 t_A}{2}$ can be represented by $\omega_0 t_C$. Hence, (3.15) can be rewritten as

$$I_E - I_A = \sqrt{2}\omega_0 T_s I_{ref} \cos(\omega_0 t_C) \tag{3.16}$$

Substituting (3.10) and (3.16) into (3.14) to yield

$$d_i = \frac{\sqrt{2} L \omega_0 I_{ref} \cos(\omega_0 t_C) + \sqrt{2} V_g \sin(\omega_0 t_C)}{V_{dc}} \tag{3.17}$$

where t_C can be represented by $(iT_s - 0.5T_s)$.

However, the calculation of the peak current ripple can be simplified through using d_i to represent $\frac{I_E - I_A}{T_s}$. Combining (3.13) and (3.14), ΔI_{p_i} can be formulized as

$$\Delta I_{p\_i} = (V_{dc} - d_i V_{dc}) \cdot \frac{d_i T_s}{4L} \tag{3.18}$$

Then, Substituting (3.18) into (3.8), the RMS value of current ripples over a fundamental period can be expressed as (3.19).

$$\Delta I_{g\_RMS} = \frac{V_{dc} T_s C_1}{4\sqrt{3}L} \sqrt{\frac{2}{N} \sum_{i=1}^{N/2} (C_2{}^2 - 2C_1 C_2{}^3 + C_1{}^2 C_2{}^4)} \tag{3.19}$$

where

$$\begin{cases} C_1 = \frac{\sqrt{2V_g{}^2 + 2(L\omega_0 I_{ref})^2}}{V_{dc}} \\ C_2 = \sin(iT_s\omega_0 - 0.5T_s\omega_0 + \varphi) \\ \varphi = \tan^{-1}\frac{L\omega_0 I_{ref}}{V_g} \end{cases} \tag{3.20}$$

Furthermore, since the switching frequency is much higher than the grid frequency, (3.19) can be rewritten by integrating the RMS value of current ripples of every switching period

$$\Delta I_{g\_RMS} = \frac{V_{dc} T_s C_1}{4\sqrt{3}L} \sqrt{\frac{1}{\pi} \int_0^{\pi} (C_2{}^2 - 2C_1 C_2{}^3 + C_1{}^2 C_2{}^4)\, d(\omega_0 t)} \tag{3.21}$$

Solve (3.21) to obtain an estimation of the RMS current ripple of the output grid current (see Appendix C for detail calculations)

$$\begin{aligned} \Delta I_{g\_RMS} = {} & \frac{T_s}{24\sqrt{2\pi}LV_{dc}} \cdot [36\pi V_g{}^4 + 72\pi V_g{}^2 \left(L\omega_0 I_{ref}\right)^2 + 36\pi \left(L\omega_0 I_{ref}\right)^4 + \\ & 24\pi V_{dc}{}^2 V_g{}^2 + 24\pi V_{dc}{}^2 \left(L\omega_0 I_{ref}\right)^2 - 128\sqrt{2} V_{dc} V_g{}^3 - 192\sqrt{2} V_{dc} V_g \left(L\omega_0 I_{ref}\right)^2]^{\frac{1}{2}} \end{aligned} \tag{3.22}$$

3.3.2 THD/ TDD Estimation Model Based on Current Ripples

As discussed in Section 3.2, equations (3.6a) and (3.6b) describe the relationship between the THD and TDD of the output grid current and the corresponding current ripples,

respectively. For calculation of the current THD, the magnitude of the fundamental component of the grid current I_1 can be represented by the RMS value of the reference current I_{ref}. Thus, substituting (3.22) into (3.6a), the current THD can be estimated by

$$\mathrm{THD}_{est} = \frac{\Delta I_{g\_RMS}}{I_{ref}} = \frac{T_s}{24\sqrt{2\pi}LV_{dc}I_{ref}} \cdot \left[36\pi {V_g}^4 + 72\pi {V_g}^2 \left(L\omega_0 I_{ref}\right)^2 + 36\pi \left(L\omega_0 I_{ref}\right)^4 + 24\pi {V_{dc}}^2 {V_g}^2 + 24\pi {V_{dc}}^2 \left(L\omega_0 I_{ref}\right)^2 - 128\sqrt{2} V_{dc} {V_g}^3 - 192\sqrt{2} V_{dc} V_g \left(L\omega_0 I_{ref}\right)^2\right]^{\frac{1}{2}} \quad (3.23)$$

As for the current TDD estimation, the rated current (I_{rated}) is used as the maximum demand current I_m which is defined in (3.6b) and thus the estimated TDD model can be expressed as

$$\mathrm{TDD}_{est} = \frac{\Delta I_{g\_RMS}}{I_m} = \frac{T_s}{24\sqrt{2\pi}LV_{dc}I_{rated}} \cdot \left[36\pi {V_g}^4 + 72\pi {V_g}^2 \left(L\omega_0 I_{ref}\right)^2 + 36\pi \left(L\omega_0 I_{ref}\right)^4 + 24\pi {V_{dc}}^2 {V_g}^2 + 24\pi {V_{dc}}^2 \left(L\omega_0 I_{ref}\right)^2 - 128\sqrt{2} V_{dc} {V_g}^3 - 192\sqrt{2} V_{dc} V_g \left(L\omega_0 I_{ref}\right)^2\right]^{\frac{1}{2}} \quad (3.24)$$

A 10 kW grid-connected single-phase inverter has been used as an experimental platform to verify the THD and TDD estimation based on the calculation of current ripples. In order to specify the current harmonic analysis in a wide frequency spectrum range, a HIOKI 8860-50 Memory Hicorder has been used for simultaneous recording of the grid current and then the Powergui Fast Fourier Transform (FFT) Analysis Tool in Matlab has been utilized to perform harmonic analysis of the collected current waveforms. The maximum frequency for harmonic analysis is 50 kHz in this research which is half the sampling frequency of the grid current by using the HIOKI 8860-50 Memory Hicorder.

Table 3.1 lists the current THD and TDD values from both the estimation and experimental results when the proposed double-frequency CCSVPWM controller with a time-delay compensator (details are discussed in Chapter 5) is applied. The switching frequency is set to be 10 kHz and the magnitude of reference voltage of the dc-link is 390 V. The harmonic analyses of the experimental current are detailed in Appendix D.

Table 3.1 Estimated and experimental THD/ TDD based on current ripples

Output Power (kW)	V_g (V)	I_{ref} (A)	I_1 (A)	Estimated Current THD_{est} (%)	Expt. Current THD (%)	Estimated Current TDD_{est} (%)	Expt. Current TDD (%)
0.98	239.5	4.2	4.60	15.52	13.21	1.56	1.29
2.07	240.2	8.4	8.51	7.77	7.48	1.57	1.53
3.07	239.8	12.5	12.75	5.21	5.08	1.56	1.55
4.03	240.5	16.7	16.39	3.90	3.89	1.56	1.53
4.95	240.6	20.8	20.31	3.13	3.12	1.56	1.52
5.99	240.4	25.0	24.82	2.60	2.67	1.56	1.59
7.07	240.5	29.2	28.69	2.23	2.33	1.56	1.60
8.05	240.2	33.3	33.03	1.95	2.05	1.56	1.62
9.04	240.5	37.5	37.25	1.73	1.84	1.56	1.64
9.83	239.9	41.0	40.37	1.58	1.69	1.55	1.64

In Table 3.1, the experimental current TDD values are obtained by definition from

$$\text{TDD} = \frac{THD \cdot I_1}{I_{rated}} \times 100\% \tag{3.25}$$

According to Table 3.1, the errors between the experimental current THD/ TDD results and the estimated values are quite small particularly when the output power is more than 3 kW, which indicates that with the proposed method, the total harmonic current can be predicted by estimating the RMS value of current ripples. However, the estimated current

harmonics with this method includes harmonic content in all frequency ranges which can be classified into two primary types of current harmonic distortions distinguished from the frequency spectrum of FFT analysis when EMI ranges are excluded:

- Low frequency harmonic component, which is typically required for grid interconnection standards to analyze and evaluate the power quality within frequency range up to 3 kHz. In this frequency range, the harmonic analysis includes up to typical 50th-order harmonic content with 60 Hz fundamental frequency [31].
- High frequency harmonic component, which is in the frequency range of more than 3 kHz and correlated with modulation frequency of switching conversion of power [108]. In this frequency range, the harmonic analysis is not normally a compulsory requirement of the grid interconnection standards and the harmonic distortions can be attenuated or even eliminated by filtering methods [109]-[111].

It is clear that low frequency harmonic distortion of the grid current is the main concern for the power quality as well as required by the grid interconnection standards, assuming high frequency harmonic contents can be eliminated by a proper low-pass filter. Hence, the low frequency harmonics are necessary to differentiate from the total harmonic contents in order to build the current THD/ TDD model specific to requirements of the grid interconnection standards.

3.3.3 THD/ TDD Estimation Model Specific to Standards Requirements

In general, the amplitudes of current harmonics decrease along with the increase of frequency. When a higher switching frequency is applied to the grid-connected inverter, the spectrum of current harmonic distortions increases towards higher frequencies and thus the quality of the power fed to the grid is improved with a lower current THD/ TDD value. However, for high frequency current harmonics, the maximum distortions are usually observed around the carrier frequency of corresponding PWM. Fig 3.5(a) shows a harmonic analysis by the FFT Analysis Tool of Matlab for the grid current with an 8 kW output power, where 0.467 V respects the maximum amplitude of the fundamental current coming from a Tektronix A622 current probe with the 10 mV/A range which is 46.7 A. It is clear that the current harmonics concentrate both in the low frequency range and around 20 kHz which is the frequency of actual switching behaviors under the double-frequency CCSVPWM control. Thus, the low frequency harmonic distortion can be evaluated by deducting the high frequency harmonic component from all possible current harmonics.

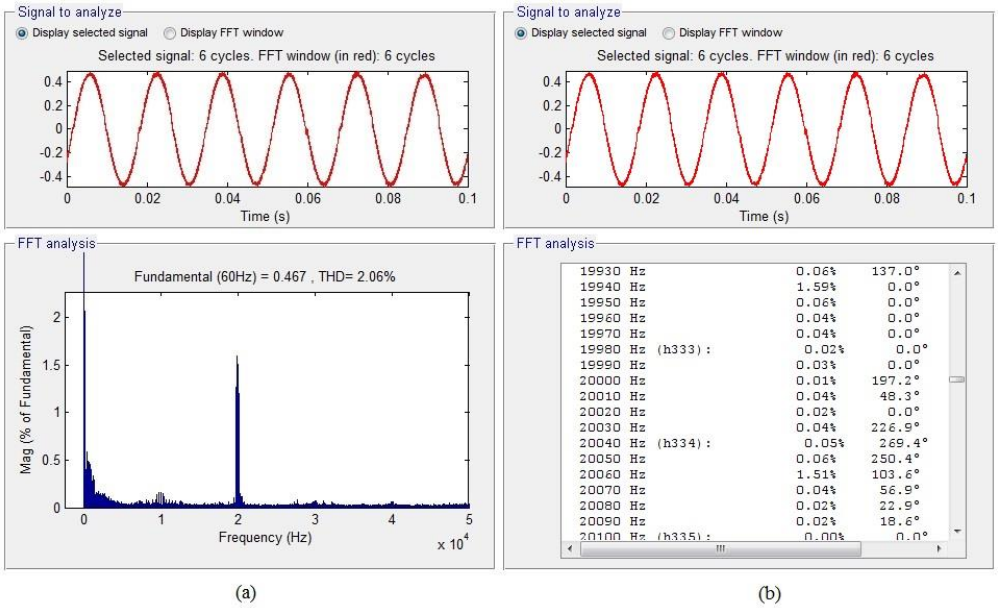


Fig. 3.5Harmonic analysis of grid current at 8 kW (a) harmonic spectrum (b) harmonic magnitudes at around 20 kHz

According to the double Fourier series approach described in [112], the current harmonics in the high frequency range primarily appear at frequencies $f = nf_0 + mf_c$, $m = 1, n = \pm1, \pm2, \pm3$, where f_c is the frequency of switching behaviors and f_0 is the grid frequency. In particular, the dominant component of all high frequency harmonic distortions is proven to locate at the frequency $f = f_c \pm f_0$ for the proposed modulation technique, which can also be seen from Fig. 3.5(b). As a result, a method where high frequency harmonic content is estimated by calculating the amplitude of the harmonic distortion at frequency $f = f_c \pm f_0$ is proposed in this dissertation.

As shown in Fig. 2.8 in Chapter 2, an L filter is used for the proposed VSI topology. In order to make it easier to calculate the current harmonic content at a specific frequency,

an equivalent circuit for the harmonics is built as shown in Fig. 3.6, where $V_{ab\_h}(f)$ and $X_L(f)$ represent the amplitude of the harmonic voltage of the inverter output and the impedance of the inductor at the frequency f, respectively. Here, $V_g(f)$ is the grid voltage and its harmonics are assumed to be zero. Hence, the RMS value of current harmonic component appearing at the frequency f can be obtain by

$$I_{g\_h}(f) = \frac{V_{ab\_h}(f)}{\sqrt{2}X_L(f)} \tag{3.26}$$

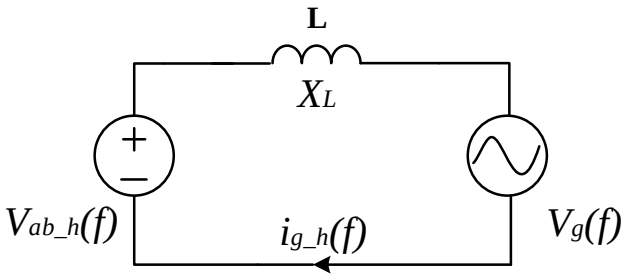


Fig. 3.6 Equivalent circuit for harmonics of VSIs

A typical waveform of the voltage across the inductor under CCSVPWM control is shown in Fig. 3.3(a). Due to the zero harmonic content of the grid voltage, only the output voltage of the inverter (v_{ab}) which is shown in Fig.3.7 contributes to the harmonic component of the inductor voltage. Furthermore, since the waveform of v_{ab} with a proper CCSVPWM control has the property of half-wave symmetry when the switching frequency is much higher than the fundamental frequency, a_{00} and a_{mn} are zeros and the amplitudes of the harmonic voltage of v_{ab} at the frequencies $f = f_c \pm f_0$ can be represented based on the double Fourier series theory by

$$V_{ab\_h}(f_c \pm f_0) = b_{11} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} v_{ab}(\omega_0 t, \omega_s t)\sin(\omega_0 t + \omega_s t)\, d\omega_s t d\omega_0 t \qquad (3.27)$$

where $\omega_0 = 2\pi f_0$ and $\omega_s = 2\pi f_c = 4\pi f_s$. f_s is the switching frequency, which is half of the frequency of switching behaviors for the double-frequency CCSVPWM algorithm.

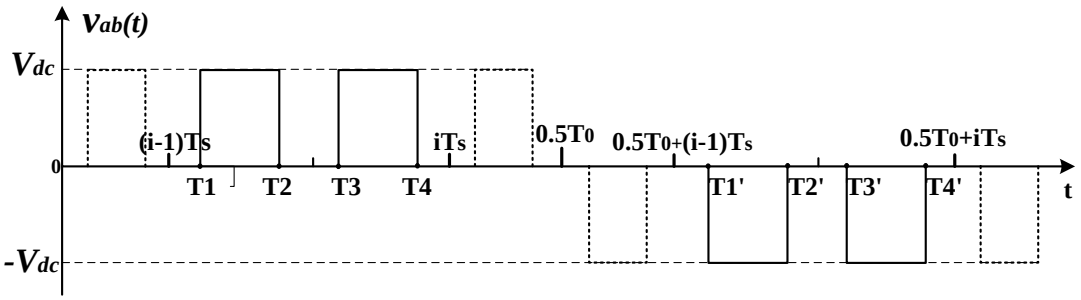


Fig. 3.7 Waveform of output voltage of inverters

According to the waveform of v_{ab} shown in Fig. 3.7, (3.27) can be rewritten as

$$b_{11} \cong \frac{1}{\pi^2}\sum_{i=1}^{K}\Big[\int_{(i-1)\frac{4\pi\omega_0}{\omega_s}}^{(i-0.5)\frac{4\pi\omega_0}{\omega_s}}\int_{\omega_s T_1}^{\omega_s T_2} V_{dc}\sin(\omega_0 t + \omega_s t)\, d\omega_s t d\omega_0 t + \int_{(i-0.5)\frac{4\pi\omega_0}{\omega_s}}^{i\frac{4\pi\omega_0}{\omega_s}}\int_{\omega_s T_3}^{\omega_s T_4} V_{dc}\sin(\omega_0 t + \omega_s t)\, d\omega_s t d\omega_0 t\Big] \qquad (3.28)$$

where K is an integer and $K \le \frac{f_s}{2f_0}$, T_s is the switching period which equals to $\frac{4\pi}{\omega_s}$, and T_1, T_2, T_3 and T_4 are determined by the duty cycle during each switching period d_i which are given by

$$\begin{cases} T_1 = (i-1)T_s + \frac{(1-d_i)}{4}T_s \\ T_2 = (i-1)T_s + \frac{(1+d_i)}{4}T_s \\ T_3 = (i-1)T_s + \frac{(3-d_i)}{4}T_s \\ T_4 = (i-1)T_s + \frac{(3+d_i)}{4}T_s \end{cases} \qquad (3.29)$$

Solve (3.28) to obtain

$$b_{11} \cong \frac{1}{\pi^2}\sum_{i=1}^{K}\left[8V_{dc}\cdot\frac{\omega_0\pi}{\omega_s}\cdot\sin(d_i\pi)\cdot\cos\frac{(\omega_s+\omega_0)(T_1+T_2-T_3-T_4)}{4}\cdot\sin\frac{(\omega_s+\omega_0)(T_1+T_2+T_3+T_4)}{4}\right] \tag{3.29}$$

As$\omega_s \gg \omega_0$,$\cos\frac{(\omega_s+\omega_0)(T_1+T_2-T_3-T_4)}{4} \approx \cos(-\pi) = -1$, and then (3.29) is reformulated as

$$\begin{aligned} b_{11} &\approx \frac{1}{\pi^2}\sum_{i=1}^{K}\left[-8V_{dc}\cdot\frac{\omega_0\pi}{\omega_s}\cdot\sin(d_i\pi)\cdot\sin\frac{(\omega_s+\omega_0)\cdot 2\pi(2i-1)}{\omega_s}\right] \\ &= \frac{1}{\pi^2}\sum_{i=1}^{K}\left\{-8V_{dc}\cdot\frac{\omega_0\pi}{\omega_s}\cdot\sin(d_i\pi)\cdot\sin\left[\frac{\omega_0\cdot 2\pi(2i-1)}{\omega_s}+2\pi(2i-1)\right]\right\} \\ &= \frac{1}{\pi^2}\sum_{i=1}^{K}\left[-8V_{dc}\cdot\frac{\omega_0\pi}{\omega_s}\cdot\sin(d_i\pi)\cdot\sin\frac{2\pi\omega_0(2i-1)}{\omega_s}\right] \end{aligned} \tag{3.30}$$

Meanwhile, for small-scale VSIs, $L\omega_0 I_{ref} \ll V_g$, hence, the duty cycle d_i can be represented based on equation (3.17) by

$$d_i = \frac{\sqrt{2}V_g}{V_{dc}}\sin\frac{(2i-1)\cdot 2\pi\omega_0}{\omega_s} \tag{3.31}$$

Substitute (3.31) into (3.30) to yield

$$b_{11} \approx \frac{1}{\pi^2}\sum_{i=1}^{K}\left[-8V_{dc}\cdot\frac{\omega_0\pi}{\omega_s}\cdot\sin\left(\frac{\sqrt{2}V_g\pi}{V_{dc}}\sin\frac{(2i-1)\cdot 2\pi\omega_0}{\omega_s}\right)\cdot\sin\frac{2\pi\omega_0(2i-1)}{\omega_s}\right] \tag{3.32}$$

Note that $\frac{(2i-1)\cdot 2\pi\omega_0}{\omega_s} \in [0,\pi]$ and $\omega_s \gg \omega_0$. Thus, (3.32) can be rewritten by an integral form of

$$b_{11} \approx \frac{-8V_{dc}\omega_0}{\pi\omega_s} \cdot \frac{1}{\omega_0 T_s} \int_0^{\pi} \sin\left(\frac{\sqrt{2}V_g\pi}{V_{dc}} \sin x\right) \cdot \sin x \, dx \tag{3.33}$$

See Appendix E to obtain the solution of (3.33) by using a Taylor series

$$b_{11} \approx \frac{-2V_{dc}}{\pi} J_1\left(\frac{\sqrt{2}V_g\pi}{V_{dc}}\right) \tag{3.34}$$

where $J_1(z)$ is the Bessel function of the first kind [113].

Since the fluctuation of the grid voltage is limited to $\pm 10\%$ by standards and over-modulation control is prevented by the proposed control algorithm, $J_1\left(\frac{\sqrt{2}V_g\pi}{V_{dc}}\right)$ can be obtained by a curve fitting method which is given as

$$J_1\left(\frac{\sqrt{2}V_g\pi}{V_{dc}}\right) \cong -\frac{\sqrt{2}V_g}{V_{dc}} + 1.3 \tag{3.35}$$

Substituting (3.35) into (3.34), the amplitudes of the voltage harmonic content across the inductor at the frequencies $f = f_c \pm f_0$ is estimated by

$$b_{11} \approx \frac{2\sqrt{2}V_g - 2.6V_{dc}}{\pi} \tag{3.36}$$

Thereafter, the RMS values of current harmonic components at the frequencies $f = f_c \pm f_0$ are obtained from (3.26) as

$$I_{g\_h}(f_c \pm f_0) = \frac{2\sqrt{2}V_g - 2.6V_{dc}}{2\sqrt{2}\pi^2(2f_s \pm f_0)L} \tag{3.37}$$

As a matter of fact, the current harmonics at the frequencies $f = f_c \pm f_0$ can be seen as the dominant part which contributes to the high frequency harmonic distortion of the output current. And thus, the low frequency distortion as the primary concern of power quality can be predicted by deducting the high frequency current harmonics from all harmonic content, which is given by

$$\begin{cases} \mathrm{THD}_{Std\_est} = \dfrac{\sqrt{\Delta I_{g\_RMS}{}^2 - I_{g\_h}(f_c+f_0)^2 - I_{g\_h}(f_c-f_0)^2}}{I_{ref}} \\ \mathrm{TDD}_{std\_est} = \dfrac{\sqrt{\Delta I_{g\_RMS}{}^2 - I_{g\_h}(f_c+f_0)^2 - I_{g\_h}(f_c-f_0)^2}}{I_m} \end{cases} \tag{3.38}$$

Recalling that $2f_s \gg f_0$, (3.38) can be simplified as

$$\begin{cases} \mathrm{THD}_{Std\_est} = \dfrac{\sqrt{\Delta I_{g\_RMS}{}^2 - 2\cdot\left(\frac{2\sqrt{2}V_g - 2.6V_{dc}}{4\sqrt{2}\pi^2 f_S L}\right)^2}}{I_{ref}} \\ \mathrm{TDD}_{std\_est} = \dfrac{\sqrt{\Delta I_{g\_RMS}{}^2 - 2\cdot\left(\frac{2\sqrt{2}V_g - 2.6V_{dc}}{4\sqrt{2}\pi^2 f_S L}\right)^2}}{I_m} \end{cases} \tag{3.39}$$

Then, substituting (3.22) into (3.39), the estimated current THD/ TDD values which are expected to evaluate the power quality by the grid interconnection standards can be given by

$$\mathrm{THD}_{Std\_est} = \frac{T_S}{24\sqrt{2}\pi^2 L V_{dc} I_{ref}} \cdot \Big[36\pi^4 {V_g}^4 + 72\pi^4 {V_g}^2 \left(L\omega_0 I_{ref}\right)^2 + 36\pi^4 \left(L\omega_0 I_{ref}\right)^4 + (24\pi^4 - 576){V_{dc}}^2 {V_g}^2 + 24\pi^4 {V_{dc}}^2 \left(L\omega_0 I_{ref}\right)^2 + 748.8\sqrt{2}{V_{dc}}^3 V_g - 486.72{V_{dc}}^4 - 128\sqrt{2}\pi^3 V_{dc} {V_g}^3 - 192\sqrt{2}\pi^3 V_{dc} V_g \left(L\omega_0 I_{ref}\right)^2\Big]^{\frac{1}{2}} \tag{3.40a}$$

$$\mathrm{TDD}_{Std\_est} = \frac{T_s}{24\sqrt{2}\pi^2 L V_{dc} I_m} \cdot \Big[36\pi^4 {V_g}^4 + 72\pi^4 {V_g}^2 \big(L\omega_0 I_{ref}\big)^2 + 36\pi^4 \big(L\omega_0 I_{ref}\big)^4 + (24\pi^4 - 576){V_{dc}}^2 {V_g}^2 + 24\pi^4 {V_{dc}}^2 \big(L\omega_0 I_{ref}\big)^2 + 748.8\sqrt{2}{V_{dc}}^3 V_g - 486.72{V_{dc}}^4 - 128\sqrt{2}\pi^3 V_{dc} {V_g}^3 - 192\sqrt{2}\pi^3 V_{dc} V_g \big(L\omega_0 I_{ref}\big)^2\Big]^{\frac{1}{2}} \quad (3.40b)$$

In order to verify the accuracy of the estimated THD value by the proposed method, the current THD of a 10 kW single-phase inverter was measured by a FLUKE 43B power quality analyzer which provides a complete harmonics profile up to the 51st harmonic as well as is calibrated for the evaluation of the inverter compliance with grid interconnection standards. Fig. 3.8 shows the THD measurements under the CCSVPWM control which are summarized in the Table 3.2.

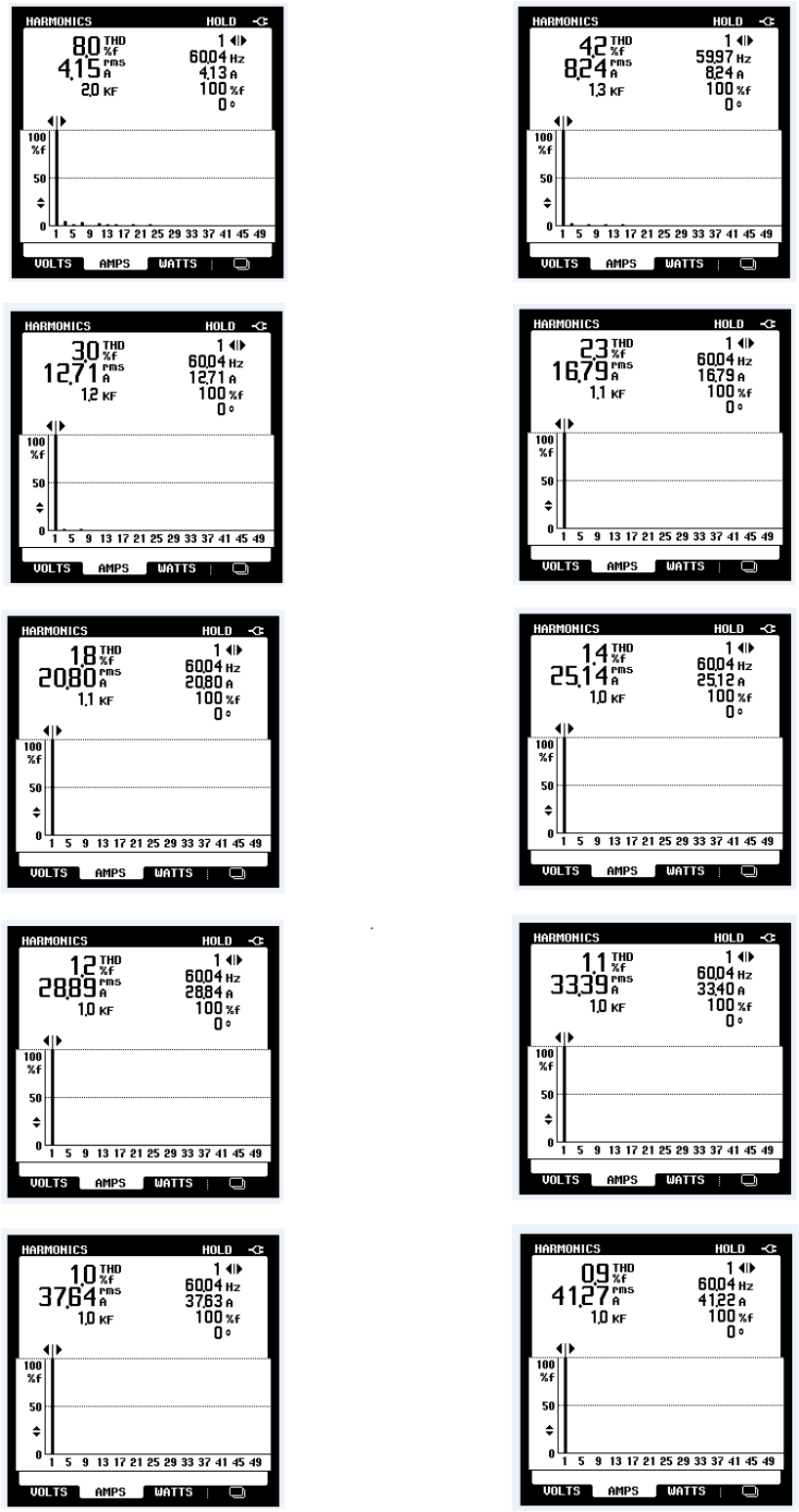


Fig. 3.8 THD measurement of a 10 kW inverter

Table 3.2 Estimated and experimental THD/ TDD based on standards requirements

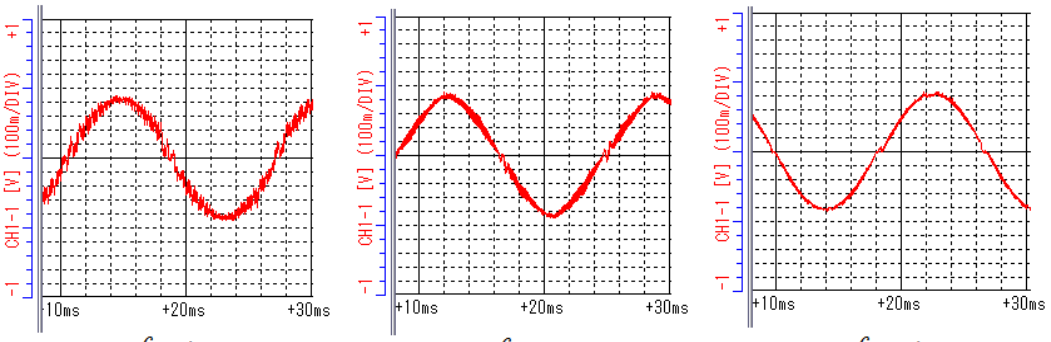
Output Power (kW)	V_g (V)	I_{ref} (A)	I_1 (A)	Estimated Current THD_{est} (%)	Expt. Current THD (%)	Estimated Current TDD_{est} (%)	Expt. Current TDD (%)
0.99	239.5	4.2	4.13	9.01	8.0	0.91	0.80
1.99	239.9	8.4	8.24	4.50	4.2	0.91	0.83
3.04	239.6	12.5	12.71	3.02	3.0	0.91	0.92
4.03	239.4	16.7	16.79	2.26	2.3	0.91	0.93
4.99	239.6	20.8	20.80	1.81	1.8	0.90	0.90
6.04	239.8	25.0	25.12	1.51	1.4	0.91	0.84
6.97	239.7	29.2	28.84	1.29	1.2	0.90	0.83
8.02	239.9	33.3	33.40	1.13	1.1	0.90	0.88
9.07	240.5	37.5	37.63	1.00	1.0	0.90	0.90
9.95	240.5	41.5	41.22	0.90	0.9	0.90	0.89

From Table 3.2, it is observed that the experimental THD/ TDD including the current harmonics up to 51st-order frequency are consistent with the estimated values which are obtained through deducting the high frequency harmonic component from current ripples. This result validates the effectiveness and accuracy of the proposed method in evaluating the current THD/ TDD under the requirements of the grid interconnection standards.

3.4 Determining Factors in THD/ TDD Performance

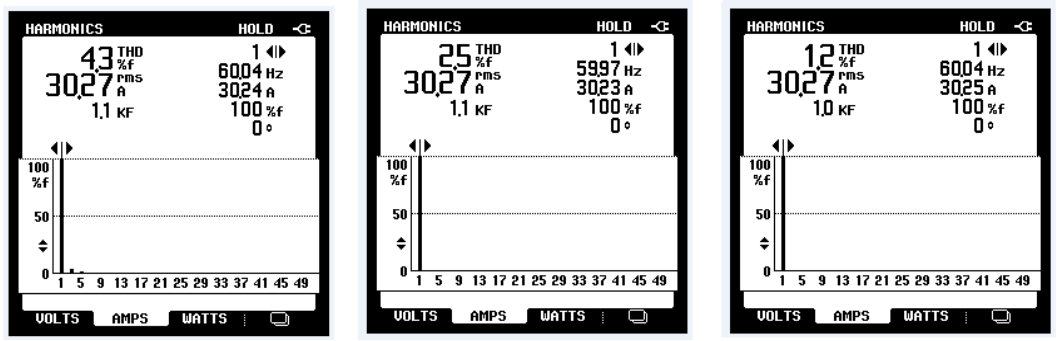
Modeling harmonic distortion of the grid current generated from VSIs is complicated and is dependent on many factors such as control algorithms, modulation techniques, power electronics devices and so on. However, the switching frequency is undoubtedly the one which has a direct impact on current THD/ TDD performance, especially with the same design of VSIs. In this chapter, a standard-based THD/ TDD estimation models under

CCSVPWM control are given as equation (3.40) and it is evident that the switching frequency is almost inversely proportional to the harmonic distortion. Fig. 3.9 gives the comparative THD measurements of 30 A grid current operated with the switching frequencies of 3 kHz, 5 kHz and 10 kHz, respectively, when the other parameters are the same. The corresponding estimated THD values by the proposed model are 4.17%, 2.50% and 1.25%.



f_S=3 kHz f_S=5 kHz f_S=10 kHz

(a)



f_S=3 kHz f_S=5 kHz f_S=10 kHz

(b)

Fig. 3.9 THD measurement with different switching frequencies when $I_g = 30$ A (a) waveforms of grid current (b) THD of grid current

Not only does the experimental result shown in Fig. 3.9 validate the proposed method in predicting the standard-based THD yet again, but also it illustrates that the current quality can be improved significantly by a higher switching frequency, achieving a lower current harmonic distortion. In other words, increasing the switching frequency of a grid-connected VSI is an effective way to reduce the harmonic content of the grid current.

However, when the same switching frequency is applied, the variations of some system variables during the operation of VSIs, such as DC-link voltage, or grid voltage, would also effect change in the current harmonic distortion. Fig. 3.10 shows the THD measurements when the grid voltage is changed. With the same switching frequency, the current THD is reduced slightly by a lower grid voltage. Although the fluctuation of the grid voltage is limited by standards, its influence on the current harmonics cannot be overlooked.

Additionally, the current THD not TDD is also determined by the output power by definition. From Table 3.2, it can be seen that the THD of the grid current reduces along with an increase in the reference current. Thus, for a given grid-connected VSI, the TDD would not vary a lot with the output power, while the THD would.

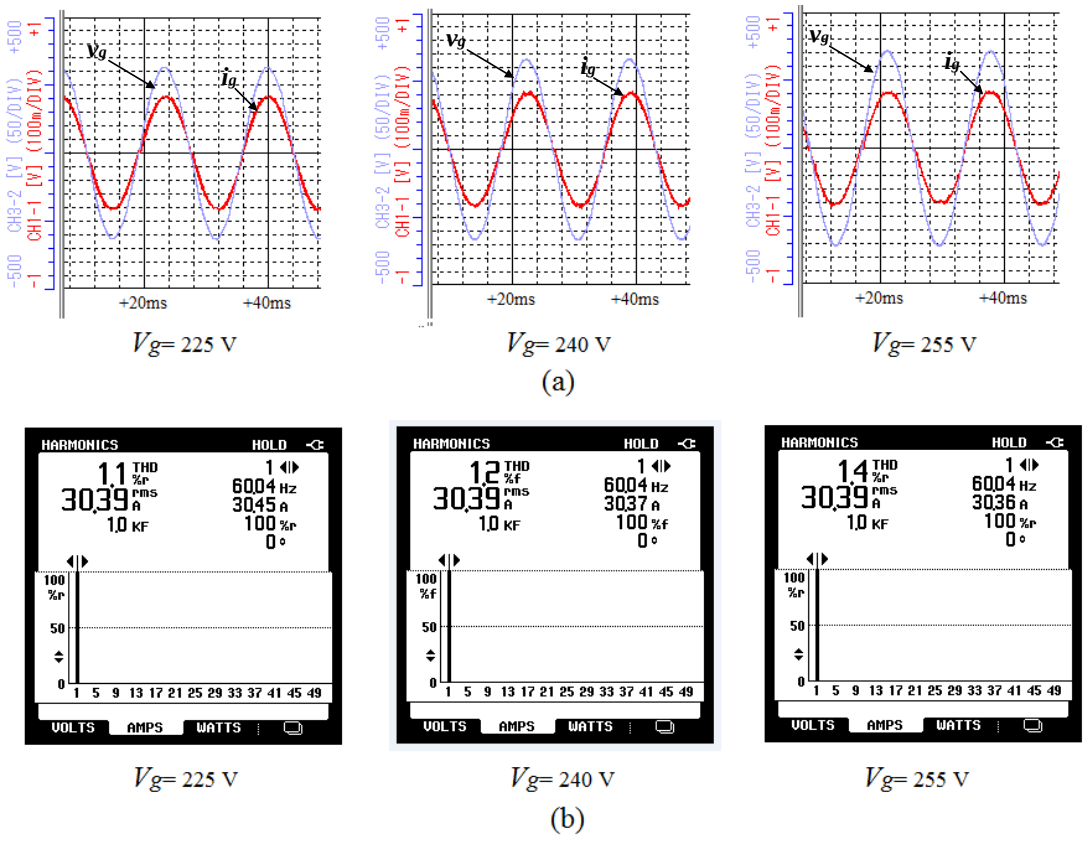


Fig. 3.10 THD measurement with variable grid voltage when $I_g = 30$ A (a) waveforms of grid voltage and current (b) THD of grid current

3.5 Summary

The current harmonic distortion of grid-connected VSIs is an important component of power quality and is a main concern of utility distribution networks required to comply with THD/ TDD requirements of the grid interconnection standards. In this chapter, a method for predicting current harmonic distortion is proposed based on the superposition theory. The current harmonics are thought to derive from ripple current and estimated by the RMS value of a sum of current ripples.

However, the harmonic contents estimated by this ripple-based method include the current harmonics in all frequency range, primarily composed of two groups: high frequency harmonic components and low frequency harmonic components. The high frequency harmonics are normally attenuated or even eliminated by filtering methods. The low frequency component of current harmonics, as the main concern for compliance with standards, can be identified by deducting the high frequency harmonics from all harmonic content obtained from the current ripple estimation. Accordingly, current THD/ TDD prediction models based on the low frequency harmonics estimation are built to satisfy the requirements of standards and experimental verified on a 10 kW single-phase grid-connected inverter under double-frequency CCSVPWM control.

According to both the expression of the THD/ TDD models and experimental results, the switching frequency of a grid-connected VSI has significant impact on current harmonic distortion, where a higher switching frequency results in a lower current harmonic distortion. In addition, the influence of other variables, such as DC-link voltage or grid voltage, cannot be neglected for predicting the THD/ TDD of the grid current.

4 A Novel Variable Switching Frequency Algorithm to Improve the Efficiency of Single-Phase Grid-Connected Inverters

4.1 Introduction

An optimal switching frequency of grid-connected VSIs is vitally important for both the efficiency of power conversion and the power quality. On the one hand, a higher switching frequency increases switching losses which are major losses of VSIs, thereby reducing the efficiency. On the other hand, a lower switching frequency results in lower power quality, in particular a higher current harmonic distortion. Thus, the selection of the switching frequency of VSIs is usually considered as a tradeoff between reducing the switching losses and achieving an optimal current harmonic performance.

In this Chapter, a novel control algorithm, called variable switching frequency control, is developed to improve both the maximum and the overall efficiencies of grid-connected VSIs through selecting optimal switching frequencies in real time under various operation conditions while meeting current THD or TDD requirement specified by grid interconnection standards. The proposed VSFC algorithm has been implemented to improve the efficiency of a 10 kW single-phase grid-connected inverter, and verified by both computer simulation and laboratory demonstration as reported in this Chapter.

4.2 Standards Overview

With increasing penetration of DGs, in particular renewable generation systems, governments and grid operators have to face new challenges related to the grid interconnection issues due to the presence of a large number of grid-connected generation systems. Thus, there is an ongoing global effort to define standards that establish requirements for interconnection of distribution resources to the utility grid in order to maintain the safety and reliability of the grid network. The main standards reviewed in this Section include CSA 22.2 No. 107.1-01 [114] – *"General Use Power Supplies"* referred to as a Canadian standard for low voltage DGs, UL 1741 [69] – *"Standard for Inverters, Converters, Controllers and Interconnection System Equipment for Use With Distributed Energy Resources"* as a dominant standard for inverter testing in the U.S., IEEE 1547 [68] – *"IEEE Standards for Interconnecting Distributed Resources with Electric Power Systems"* which is the most influential standard in North America laying the foundations for CSA 22.2 No. 107.1-01 and UL 1741, AS 4777 [70] – *"Grid Connection of Energy Power Systems via Inverters"* widely adopted in China, Australia and New Zealand, and the IEC 61727 [115] – *"Photovoltaic (PV) Systems - Characteristics of the Utility Interface"* which is an international standard specific to low voltage and low rating grid-connected PV systems. The table below outlines the aggregate capacity and grid type to which the requirements specified by each of the standards are applicable.

Table 4.1 Capacity and grid type covered by each standard

Standard Name	Aggregate Capacity	Grid Type
CSA 22.2 No. 107.1-01	Unspecified	Low voltage grids (≤ 600 V)
UL 1741	Unspecified	Unspecified
IEEE 1547	≤ 10 MVA	Distribution systems 0.12-161 kV
AS 4777	≤ 10 kVA per phase	General low voltage grids
IEC 61727	≤ 10 kVA	General low voltage grids

Most standards provide requirements relevant to the performance, operation, testing, safety, and maintenance of the interconnection [68], [116]. Since all standards cannot be covered here, the focus of this section is power quality, in particular the harmonic distortion of the DG current fed to the grid. A comprehensive summary of the current distortion limit and individual harmonics requirement for utility-interactive inverters specified by most of widespread acceptance standards can be found in Table 4.2.

Table 4.2 Current distortion limits specified by major standards

Standard	Distortion limit (%)							
	TDD	THD	Individual harmonic order					
				2nd - 9th	10th - 15th	16th - 21st	22nd - 33rd	above 33rd
CSA 22.2 No. 107.1		5.0	Odd order	4.0	2.0	1.5	0.6	0.3
			Even order	1.0	0.5	0.4	0.2	0.1
IEEE 1547	5.0		Odd order	4.0	2.0	1.5	0.6	0.3
			Even order	1.0	0.5	0.375	0.15	0.075
UL 1741		5.0	Odd order	4.0	2.0	1.5	0.6	0.3
			Even order	1.0	0.5	0.375	0.15	0.075
AS 4777		5.0	Odd order	4.0	2.0	1.5	0.6	
			Even order	1.0	0.5	0.5	0.5	
IEC 61727		5.0	Odd order	4.0	2.0	1.5	0.6	
			Even order	1.0	0.5	0.375	0.15	

According to the reviews of the major standards, the IEEE 1547 specifies a current TDD requirement with an allowance of 5% of the rated current, while most of others, particularly those required for small-scale DGs, state 5% THD as the maximum current distortion limit. Furthermore, each individual current harmonic in the low frequency range is also limited by these standards, though the detail values are slightly different.

4.3 VSFC Algorithm

4.3.1 Optimal Switching Frequency Selection

As discussed in both Chapter 2 and Chapter 3, the selection of the switching frequency for a single-phase grid-connected VSI is considered as a tradeoff between the efficiency improvement and the output quality optimization – A higher switching frequency would attenuate the current distortion, but on the other hand result in a lower efficiency. Thus, the choice of switching frequency is a key issue for grid-connected VSIs both to achieve high efficiency operation and to satisfy the requirement of grid interconnection standards related to power quality. Traditionally, a given fixed switching frequency is applied to VSIs according to design requirement, control algorithm development and loss consideration. However, a fixed switching frequency cannot be optimal for all operations due to parameter variations. In this Chapter, a set of optimal switching frequencies of VSIs can be derived from the models of VSI efficiency and current distortion estimation proposed in Chapter 2 and Chapter 3, respectively, based on given working conditions. The optimal switching frequencies will be selected to minimize the total power losses of VSIs subject to the limits on current distortion. However, considering that the power

losses with the hardware structure shown in Fig. 2.1 are approximately linearly proportional to the switching frequency, the operational switching frequencies are only bounded by the current harmonic estimation (equation 3.40) with a current THD or TDD requirement, which can be shown as

$$f_{s\_THD}(\mathrm{THD}_{Req}) \geq \frac{1}{\mathrm{THD}_{Req}\cdot 24\sqrt{2}\pi^2 L V_{dc} I_{ref}} \cdot \Big[36\pi^4 {V_g}^4 + 72\pi^4 {V_g}^2 \big(L\omega_0 I_{ref}\big)^2 + 36\pi^4 \big(L\omega_0 I_{ref}\big)^4 + (24\pi^4 - 576){V_{dc}}^2 {V_g}^2 + 24\pi^4 {V_{dc}}^2 \big(L\omega_0 I_{ref}\big)^2 + 748.8\sqrt{2}{V_{dc}}^3 V_g - 486.72{V_{dc}}^4 - 128\sqrt{2}\pi^3 V_{dc} {V_g}^3 - 192\sqrt{2}\pi^3 V_{dc} V_g \big(L\omega_0 I_{ref}\big)^2\Big]^{\frac{1}{2}} \quad (4.1a)$$

$$f_{s\_TDD}(\mathrm{TDD}_{Req}) \geq \frac{1}{\mathrm{TDD}_{Req}\cdot 24\sqrt{2}\pi^2 L V_{dc} I_m} \cdot \Big[36\pi^4 {V_g}^4 + 72\pi^4 {V_g}^2 \big(L\omega_0 I_{ref}\big)^2 + 36\pi^4 \big(L\omega_0 I_{ref}\big)^4 + (24\pi^4 - 576){V_{dc}}^2 {V_g}^2 + 24\pi^4 {V_{dc}}^2 \big(L\omega_0 I_{ref}\big)^2 + 748.8\sqrt{2}{V_{dc}}^3 V_g - 486.72{V_{dc}}^4 - 128\sqrt{2}\pi^3 V_{dc} {V_g}^3 - 192\sqrt{2}\pi^3 V_{dc} V_g \big(L\omega_0 I_{ref}\big)^2\Big]^{\frac{1}{2}} \quad (4.1b)$$

where THD_{Req} and TDD_{Req} represent the limits of allowable THD and TDD of the current fed to the grid, respectively.

Inequality (4.1a) specifies the switching frequency range which can be implemented by VSIs to satisfy a current THD requirement, while (4.1b) shows the switching frequency range based on a current TDD limit. The minimum values in those ranges would be chosen as the optimal switching frequencies to achieve the best efficiency performance. As presented in Section 4.2, a current THD requirement specified by most international utility interconnection standards gives a more stringent evaluation of power quality for

grid-connected VSIs than TDD. Hence, the selection of optimal switching frequencies in this research is carried out based on the THD estimation model. Furthermore, in order to meet the requirement of individual current harmonic, a 3% THD limit is pre-set to keep the sufficient margins. Thus, the optimal switching frequencies of VSIs can be represented by

$$f_{s\_optimal} = \min_{\mathrm{THD}_{Req}} f_{s\_THD}(\mathrm{THD}_{Req}) = \frac{1}{3\%\cdot 24\sqrt{2}\pi^2 L V_{dc} I_{ref}} \cdot \Big[36\pi^4 {V_g}^4 + 72\pi^4 {V_g}^2 \left(L\omega_0 I_{ref}\right)^2 + 36\pi^4 \left(L\omega_0 I_{ref}\right)^4 + (24\pi^4 - 576){V_{dc}}^2 {V_g}^2 + 24\pi^4 {V_{dc}}^2 \left(L\omega_0 I_{ref}\right)^2 + 748.8\sqrt{2}{V_{dc}}^3 V_g - 486.72{V_{dc}}^4 - 128\sqrt{2}\pi^3 V_{dc} {V_g}^3 - 192\sqrt{2}\pi^3 V_{dc} V_g \left(L\omega_0 I_{ref}\right)^2\Big]^{\frac{1}{2}} \quad (4.2)$$

4.3.2 System Configuration of VSFC

Due to the uncertainty and variability of wind and solar generation, it is impossible to improve the efficiencies of grid-connected VSIs under different load power levels by a fixed switching frequency. Thus, a simple and novel control algorithm called "VSFC" has been proposed in this Ph. D. research which is developed to minimize the total power losses of VSIs at various operation conditions as well as to meet a THD requirement complied with the grid interconnection standards through selecting the optimal switching frequencies in real time.

Fig. 4.1 shows the digital control system designed for VSFC with the improved CCSVPWM, which includes the outer loop of the dc-link voltage regulation, the inner

loop of the predictive current control and the improved SVPWM technique based on the optimal switching frequency. From (4.2), the optimal switching frequency of VSIs working in the (K+1)-th grid period is determined primarily by the predictions of the averaged dc-link voltage $\bar{V}_{dc}$, the RMS value of the grid voltage V_g and the amplitude of the reference current I_{ref} in the (K+1)-th grid period, which can be represented by $\hat{\bar{V}}_{dc}(K+1)$, $\hat{V}_g(K+1)$ and $I_{ref}(K+1)$, respectively. Here $\hat{\bar{V}}_{dc}(K+1)$ can be estimated by a linear predictor with a low frequency (120 Hz) mean value filter, $\hat{V}_g(K+1)$ is assume to be the same as that in the previous grid cycle, while $I_{ref}(K+1)$ is obtained from the V_{dc} PI controller employed to balance the power flow through maintaining a constant dc-link voltage which has been discussed in Section 2.2.

$$\begin{cases} \hat{\bar{V}}_{dc}(K+1) = 2\bar{V}_{dc}(K) - \bar{V}_{dc}(K-1) \\ \hat{V}_g(K+1) = V_g(k) \\ I_{ref}(K+1) = I_{ref}(K) + K_p[\mathrm{E}_{dc}(K+1) - \mathrm{E}_{dc}(K)] + K_i T_0 \mathrm{E}_{dc}(K+1) \end{cases} \tag{4.3}$$

where $\mathrm{E}_{dc}(K) = \mathrm{V}_{dc}^{*}(K) - \hat{\bar{V}}_{dc}(K-1)$, T_0 is the sampling time which equals to the grid period; K_p and K_i are parameters of the PI controller. In this Chapter, $K_p = -0.72$ and $K_i = -0.11$, which are tuned by the typical Ziegler-Nichols frequency response method [117].

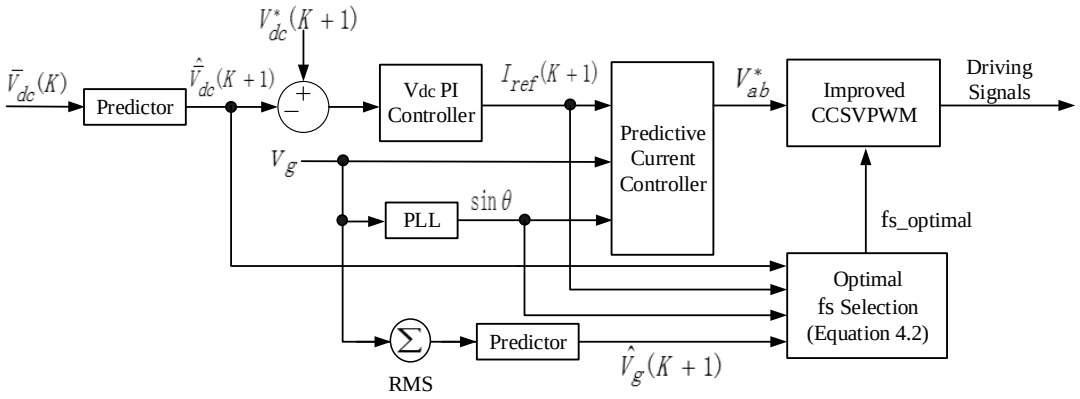


Fig. 4.1 Block diagram of VSFC

In addition, as the calculation of (4.1) needs to take few milliseconds at the computing speed of 40 million instructions per second (MIPS) by the DSP TMS320LF2407A from Texas Instruments (TI), or about one fifth of the grid period, the proposed VSFC starts working at the central point of each grid cycle in order to guarantee that there is sufficient time to calculate and update the optimal switching frequency before the beginning of the next grid cycle.

4.3.3 Predictive Current Controller Design

In the inner loop of the proposed VSFC, a predictive current controller has been developed to achieve the fast dynamic response, accurate current tracking and easy implementation on a DSP-based digital control system. There are several current control techniques presented under the name of "predictive control" in grid-connected VSI applications, such as the well-known deadbeat controller [118], [119], the Smith predictor [120], the model predictive control (MPC) methods [121], [122] and so on. In this

Chapter, the proposed predictive current controller is developed from a typical deadbeat control scheme based on the averaged switch model of VSIs. From (2.23), the averaged output voltage of the inverter (v_{ab}) can be written in discrete form as

$$v_{ab}(K+1) = L\frac{i_g(K+1)-i_g(K)}{T_s} + \overline{v_g}(K+1) \tag{4.4}$$

where T_s is the switching period, $i_g(K)$ and $i_g(K+1)$ are the grid currents measured at the end points of K-th and $(K+1)$-th switching periods, and $\overline{v_g}(K+1)$ is the averaged value of the grid voltage during the $(K+1)$-th switching period.

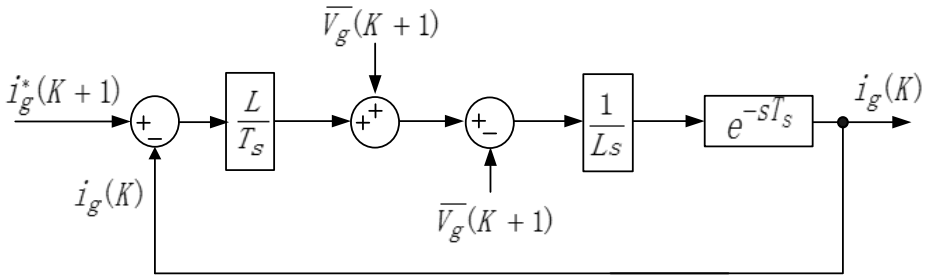


Fig. 4.2 Deadbeat control scheme of grid-connected VSIs

The deadbeat controller can be simply designed according to (4.4) if a precise model of the system is given and no extra delay time is introduced, which is shown as Fig. 4.2. Under this condition, the deadbeat controller has fast response and good tracking performance by enforcing the grid current $i_g(K+1)$ to the value of the reference current $i_g^*(K+1)$. However, in practical implementation, the delay due to sampling and calculation time is inevitable, which makes it impossible to acquire the instantaneous value of the grid current at the end point of the K-th switching period, $i_g(K)$. In order to overcome this problem, a predictive current controller is presented in this section to

compensate the delay time by forecasting the forthcoming values of system variables. As shown in Fig. 4.3, the actual values of the grid current $i_g(K)$ and the averaged grid voltage $\overline{v_g}(K+1)$ are estimated by a linear function based on the past measurements with a real-time sampling strategy, which are represented by $\hat{\imath}_g(K)$ and $\hat{\bar{v}}_g(K+1)$, respectively. And thus, the acquired (reference) output voltage of the inverter can be described by

$$v_{ab}^*(K+1) = L\frac{i_g^*(K+1)-\hat{\imath}_g(K)}{T_s} + \hat{\bar{v}}_g(K+1) \tag{4.5}$$

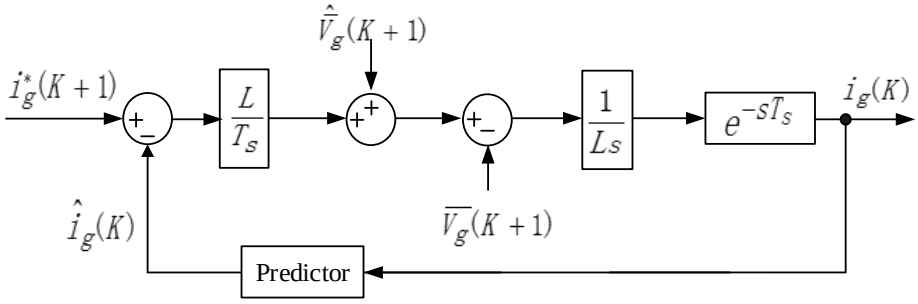


Fig. 4.3 Predictive control scheme of grid-connected VSIs

The performance of the presented predictive current controller including the output current distortion, effect of the delay time and robustness under parameter mismatches is depended heavily on the prediction methods applied to the estimation of forthcoming values of the grid current and voltage. The linear prediction technique is utilized in this Ph.D. research due to the characteristic of easy development and good robustness, i.e. no knowledge of the model of the system is required. However, the applied sampling strategy can strongly influence the accuracy of prediction.

4.3.4 Sampling Strategy for VSFC

There are several sampling schemes developed for the predictive current controller to compensate the effect of the control delay as well as minimize the current distortion in the applications of grid-connected VSIs: a dual-timer sampling strategy was presented in [123] to monitor the output current with a shorter interval, [124] proposed a real-time sampling scheme combined with a low-pass filter, and the sampling method was optimized with a fixed minimum delay time presented in [77]. All of these sampling schemes are developed based on the control system with a fixed switching frequency. When the sampling frequency in a DSP-based digital system is a constant and a multiple of the switching frequency, the distribution of sampling points in every switching period is the same. However, in VSFC, the distribution of sampling points varies in different switching periods along with the optimal selection of the switching frequency. Thus, a new sampling strategy is designed in this Section to ensure that the proposed VSFC can work properly under the condition that the sampling points are randomly distributed in a PWM period when the switching frequency is changed. Fig. 4.4 shows the time arrangement for the predictive current control implemented with DSP TMS320LF2407A, where T_{ADC} represents the sampling period, T_d refers to the inherent control delay caused by the calculation and updating of the reference value of the inverter output, and $A(K)$ and $B(K)$ are the sampling points. The sampling frequency is 40 kHz and the maximum of the switching frequency is set to 10 kHz with the improved CCSVPWM technique.

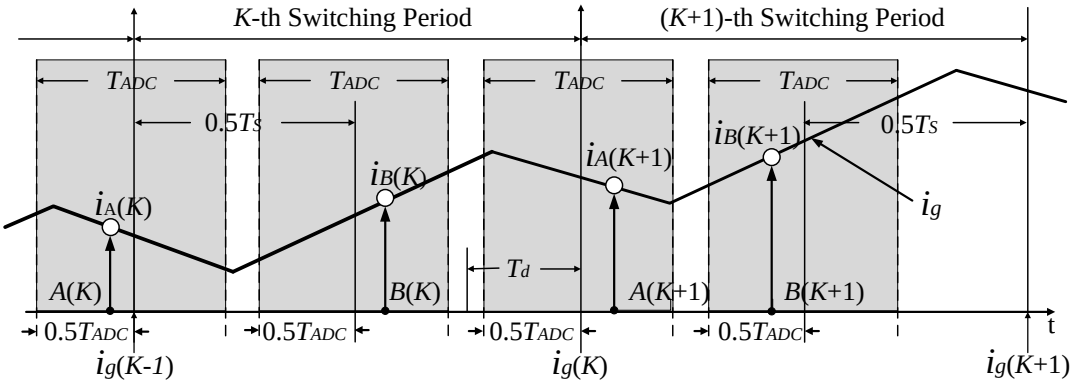


Fig. 4.4 Arrangement of sampling strategy for VSFC

As the sampling methods dependent on the fixed sampling distribution are not suitable for VSFC, the sampling strategy proposed in this Chapter is developed by building a timer which has the same time sequence as the built-in timer of the DSP and is synchronized at the initial point of each grid voltage cycle. Then, the created timer can be utilized to identify the distribution of sampling points. In Fig. 4.4, $A(K)$ is sampling point during sampling period $[(K-1)T_s - 0.5T_{ADC}, (K-1)T_s + 0.5T_{ADC}]$, which can be viewed as an approximation of the value of the actual current at $(K-1)T_s$. Thus, the current at the end of the K-th switching period can be predicted by (4.6) with symmetric PWM control.

$$\hat{\imath}_g(K) = 2i_B(K) - i_A(K) \tag{4.6}$$

where $i_A(K)$ is actual current at point $A(K)$, and $i_B(K)$ is the current measurement from the sampling point $B(K)$ in the sampling period $[(K-0.5)T_s - 0.5T_{ADC}, (K-0.5)T_s + 0.5T_{ADC})$.

In addition, assuming that the change of the grid voltage is linear in two consecutive switching periods when the switching frequency is much higher than the grid frequency, the averaged grid voltage in the $(K+1)$-th switching period as system disturbance can be estimated by

$$\hat{\bar{v}}_g(K+1) = 3v_{g\_B}(K) - 2v_{g\_A}(K) \tag{4.7}$$

where $v_{g\_A}(K)$ and v_{g_B}(K) are the grid voltage measured at the sampling points $A(K)$ and $B(K)$, respectively.

Considering that the maximum switching frequency for VSFC is 10 kHz and the sampling frequency is 40 kHz, there are at least four sampling points in a switching period. Thus, the predictive current control based on this sampling scheme has sufficient time to calculate and update the reference value of the inverter output. With the implementation of DSP TMS320LF2407A, the inherent control delay T_d is approximately 20 μs which is less than a sampling period.

4.4 Simulation and Experimental Results

To verify the proposed VSFC including the dc-link voltage regulation, the predictive current control and the optimal switching frequency selection, a simulation model in Simulink of Matlab was developed and then VSFC was implemented on a 10 kW prototype single-phase grid-connected inverter based on a DSP TMS320LF2407A. In addition, the performance of VSFC in terms of the current distortion and inverter efficiency was evaluated by comparing with two other control schemes, unipolar SPWM

control and improved CCSVPWM control without VSFC which have been discussed in Chapter 2.

4.4.1 Simulation Results

The proposed VSFC system is modeled and simulated in Simulink as shown in Fig. 4.5, where the s-function block is programmed as a SVPWM generator and the function block is constructed for the optimal switching frequency selection. Fig. 4.6 shows the dynamic response of the system under a step change of the input power at $t = 0.035$ s from 4 kW to 8 kW. As the new switching frequency and the reference current obtained from the optimal switching frequency selection and dc-link voltage regulation respectively would be updated in the next grid cycle, the current would increase to a RMS value of 33.3 A (corresponding to 8 kW) from $t = 0.0501$ s to balance the power flow. During this control process, although the switching frequency was constantly changing due to the increase of the output current as well as the variation of the dc-link voltage, the current THD is always less than the preset required value of 3%.

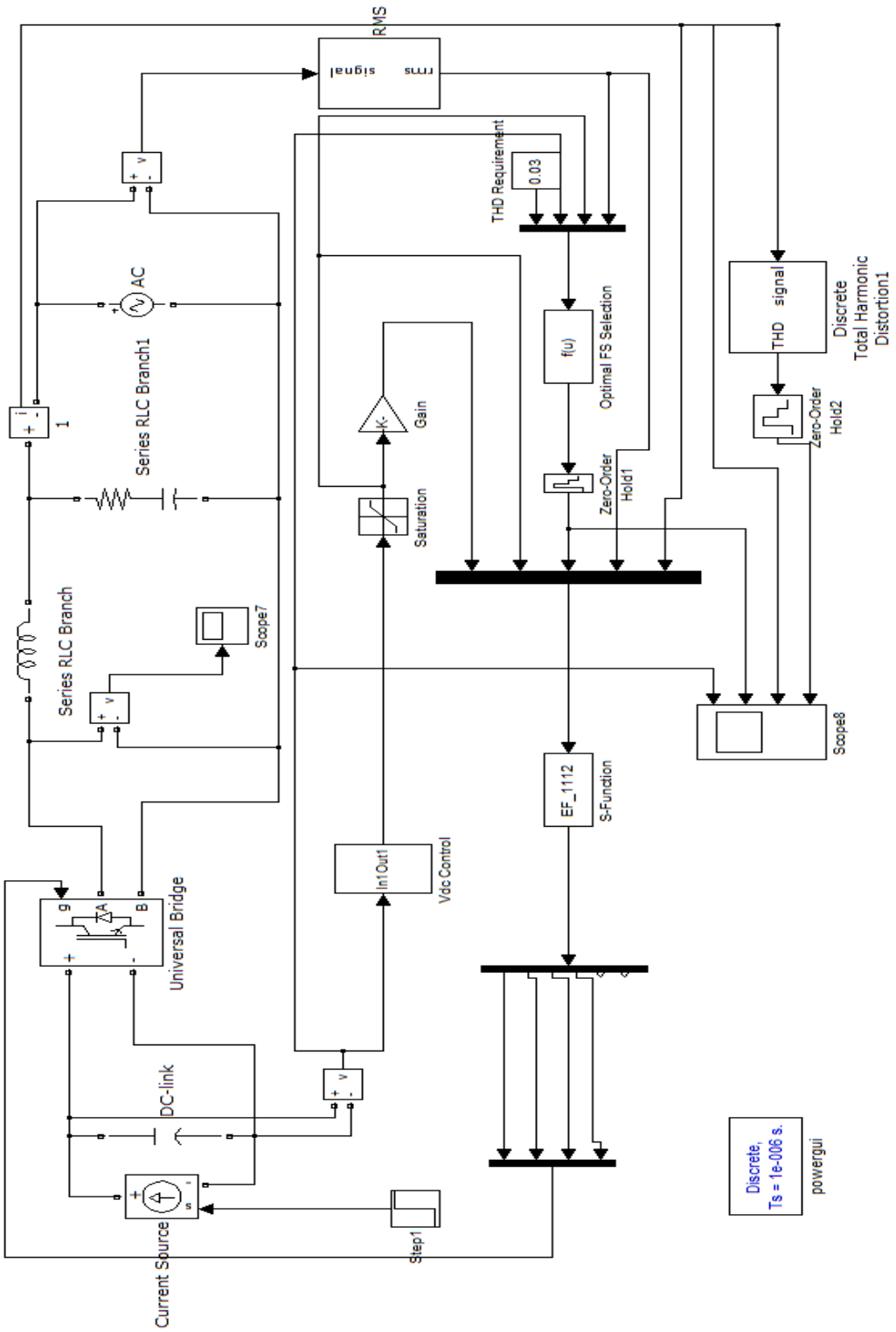


Fig. 4.5 Simulink model of VSFC

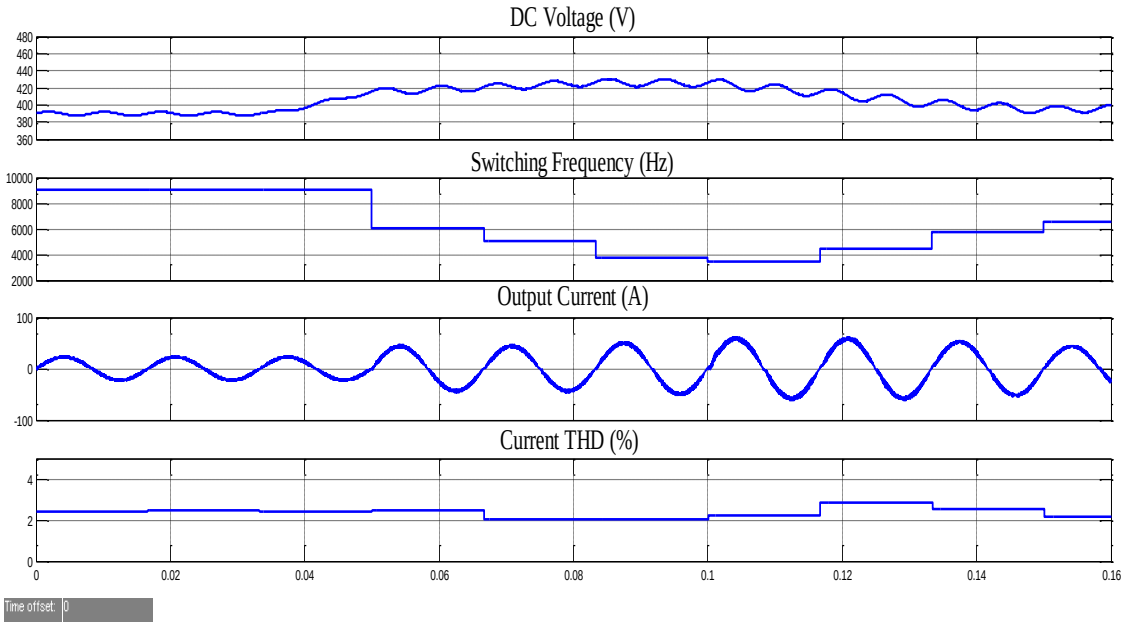


Fig. 4.6 Dynamic response with a step change of power demand

In addition, an evaluation program written in M-language is developed to compare the efficiency and THD performance of the inverter among the proposed control scheme, the modified CCSVPWM control and the conventional SPWM technique. The simulation results shown in Fig. 4.7 and Fig. 4.8 prove that compared with other two PWM techniques, the proposed VSFC is effective to improve the inverter efficiency by selecting optimal switching frequencies while ensuring the current distortion meeting the standard requirement. When a THD requirement value is set to 3%, the maximum efficiency of the inverter with VSFC is 96.27%, markedly higher than 95.28% with the other two control algorithms.

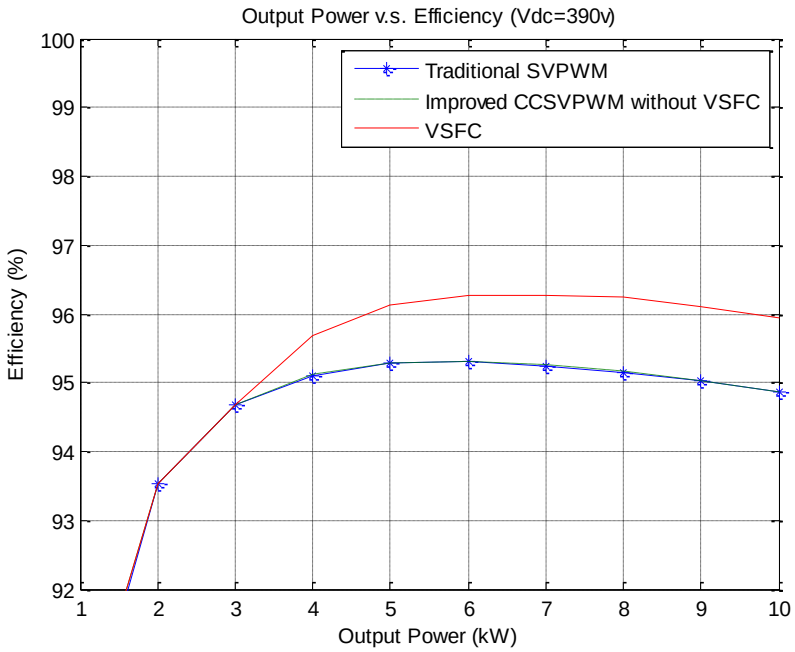


Fig. 4.7 Simulation results of inverter efficiency with different control schemes

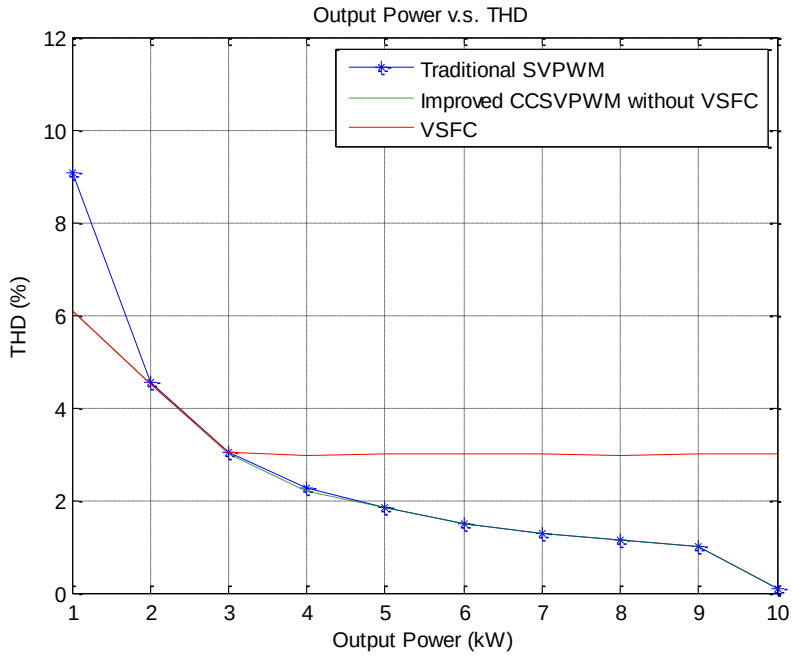


Fig. 4.8 Simulated current THD performance under different control schemes

4.4.2 Experimental Verification

The proposed control algorithm is implemented on a custom DSP board based on a 16-bit TMS320LF2407A chip and verified on a prototype 10 kW single-phase grid-connected inverter, as shown in Fig. 4.9. The prototype inverter has the same schematic diagram presented in Fig. 2.1 and the same parameters listed in Table 2.2.

Fig. 4.9 10 kW prototypical single-phase grid-connected inverter

In order to evaluate the output quality of the inverter with VSFC, a FLUKE 43B power quality analyzer has been used to record the variations of the current THD with different input power levels for four-minute operation. The maximum switching frequency of the inverter is set to 10 kHz and a 3% THD is used as the preset requirement of current distortion for the optimal switching frequency selection. These choices give a safety margin of computing time and power quality requirement from standards. In Fig. 4.10, the current THD has maintained at a lower value in the allowable range specified by the

grid interconnection standards when the current has varied during 6.28 A to 41.02 A, which proves the effectiveness of the proposed VSFC method in terms of current distortion control. Moreover, the average THD value is 3.7% from Fig. 4.10, a little bit more than the preset THD requirement, since the power analyzer cannot perform the correct THD value when the power is changed rapidly and the linear predictor used for the current control cannot completely compensate the random control delay.

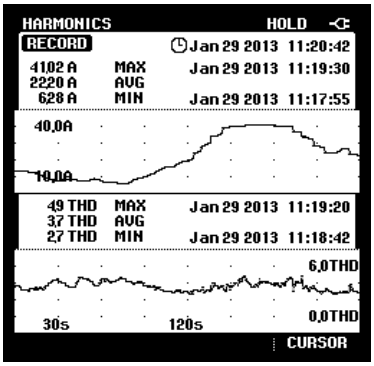
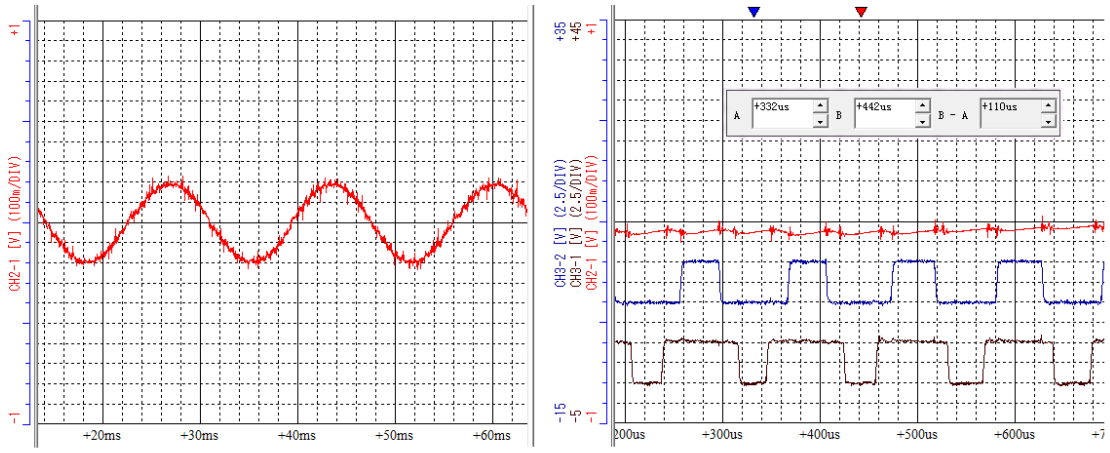


Fig. 4.10 Current THD recorded for 4-min operation with input power variations

Fig. 4.11 shows the current waveform and gate driving signals for the proposed VSFC when the inverter works at 3.3 kW and 7.5 kW, respectively. Compared with the similar and acceptable THD performance shown in Fig. 4.12, the operating switching frequencies under these two conditions are different, approximately 9 kHz at 3.3 kW and 4 kHz at 7.5 kW, which illustrates that the proposed control method can be implemented to select an optimal switching frequency for the inverter based on a real-time work condition in compliance with the THD requirement specified by standards. Table 4.3 summaries the

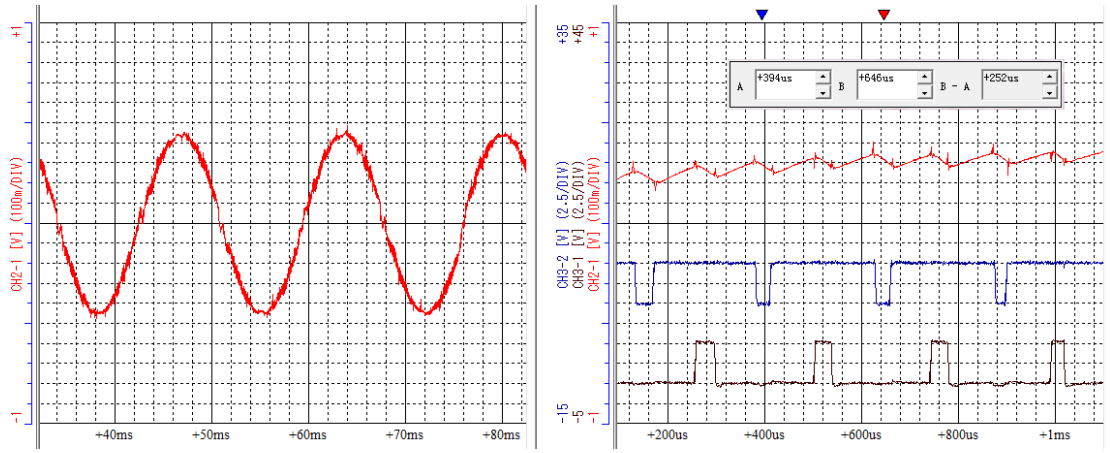
switching frequency, current THD and efficiency of the inverter operating with the proposed VSFC at different power levels.



Grid Current (10mV/A)

Grid Current (upper one), Driver Signal for IGBT 1 (medium one), Driver Signal for IGBT 4 (lower one)

(a)

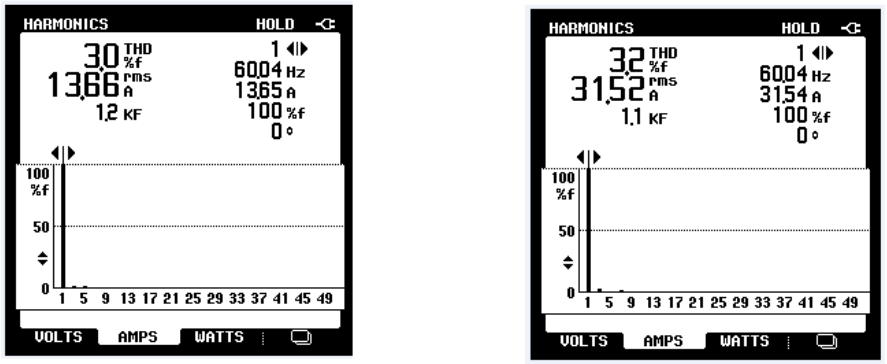


Grid Current (10mV/A)

Grid Current (upper one), Driver Signal for IGBT 1 (medium one), Driver Signal for IGBT 4 (lower one)

(b)

Fig. 4.11 Grid current waveforms and driving signals when the inverter operates with VSFC at (a) 3.3 kW (b) 7.5 kW



(a) (b)

Fig. 4.12 THD of grid current with power at 3.3 kW and 7.5 kW

Table 4.3 Switching frequency, current THD and efficiency of the inverter operating with the proposed VSFC

Output Power (kW)	**Switching Frequency (kHz)**	**Current THD (%)**	**Efficiency (%)**
1.03	10.00	9.0	89.32
2.06	10.00	4.9	93.09
2.99	9.90	3.1	94.62
5.05	6.29	3.2	95.64
7.54	3.97	3.2	96.05
9.9	2.99	3.5	95.74

For the purpose of efficiency evaluation for the inverter, the conventional unipolar SPWM technique with a switching frequency of 20 kHz and the improved CCSVPWM algorithm with a switching frequency of 10 kHz have been implemented to compare with the proposed VSFC scheme. Fig. 4.13 shows the measured inverter efficiencies working under these three methods. A significant improvement of the inverter efficiency can be observed under the proposed VSFC. Table 4.4 compares the measured efficiencies and THDs of the inverter for the different control strategies. It can be seen that under the

same requirement of current THD specified by the grid interconnection standards, the VSFC scheme proposed in this thesis can improve the maximum efficiency of the inverter for more than 0.8 percent, and European efficiency and the CEC efficiency for more than 0.5 percent in comparison to other control schemes.

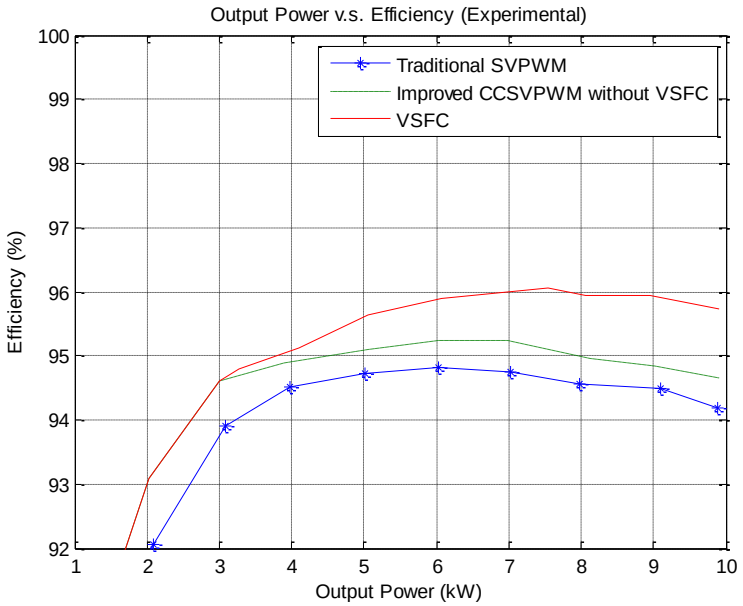


Fig. 4.13 Experimental efficiency of inverter under different control methods

Table 4.4 Efficiency and THD comparison for different control methods

	VSFC	**CCSVPWM**	**SPWM**
Frequency Range (kHz)	3 – 10	10	20
Max. Efficiency (%)	96.05	95.25	94.81
Euro. Efficiency (%)	94.40	93.91	93.41
CEC Efficiency (%)	95.38	94.77	94.24
THD of the Current (%)*	<4.9	<4.9	<4.5

*when the operationg power is equal or less than 10% of the rated power, the current THD is no longer restrictive.

4.5 Summary

Selecting an optimal switching frequency of PWM for single-phase inverters is one of the most effective ways to improve the inverters' efficiency. However, a lower switching frequency results in lower output power quality. For grid-connected inverters, the harmonic current distortion is significantly affected by the switching frequency and is upper-bounded by the grid interconnection standards. Therefore, the choice of switching frequency is usually considered as a tradeoff between obtaining a lower THD of output current and achieving a better efficiency.

In this Chapter, an overview of the most popular grid interconnection standards was presented firstly. The current THD, as one of the most important references, is widely used in power industry to evaluate the power quality for grid-connected DGs. An allowance of 3% THD was then set as a required THD value used for the current distortion estimation to ensure that there is sufficient margin to satisfy the requirement of standards in both current THD and individual harmonic distortion. Accordingly, a novel algorithm, which is called "VSFC", was developed from the estimation model of the current harmonic distortion to allow the operating switching frequency of the inverter changing along with variations of working conditions to achieve the minimum power losses bounded by the requirement of current distortion. The proposed VSFC system is composed of three major function blocks: the outer loop of the dc-link voltage regulation, the inner loop of the predictive current control and the improved SVPWM technique based on the optimal switching frequency selection. Thus, a PI dc-link controller and a predictive current controller with a time sequence sampling strategy were designed.

In addition, a simulation model and an experimental prototype of a 10 kW single-phase grid-connected inverter were built. Both simulation and experimental results verified the effectiveness of the proposed control method. An experimental efficiency analysis is also presented in this Chapter. As compared with the improved CCSVPWM and conventional SPWM techniques, the VSFC scheme can improve the maximum efficiency of the inverter by more than 0.8 percent, and European efficiency and the CEC efficiency by more than 0.5 percent.

5 An Improvement Current Controller for Single-Phase Grid-Connected Inverters with VSFC

5.1 Introduction

A predictive current controller with a novel sampling strategy is designed in Chapter 4, which offers a fast transient response, zero steady-state errors, robust time-delay compensation and full compatibility with the DSP-based digital system implementation of the proposed VSFC. However, when the inverter operates at a low or medium switching frequency, the amplified time-delay effect caused by sampling distribution, computation of the control program in DSP and inherent PWM generator update will severely degrade the system stability and dynamics as a result of the inaccurate grid current and voltage estimation by the implemented linear predictor. Moreover, the poor stability margin for parameter variations of the system model such as the practical filter inductance will also have a large influence on the performance of the predictive current controller.

In order to alleviate the aforementioned limitations, a robust current control scheme featuring high adaptability to time delays and system uncertainties and high robustness to parameter mismatch has been designed in this Chapter. The proposed scheme is built on a structure of the predictive current controller and developed with an improved time-delay compensation technique which greatly reduces the current tracking errors through a simple weighted filter prediction method and completely eliminates static voltage errors introduced by system disturbances and uncertainties through a robust adaptive voltage

compensator. Theoretical analysis and comparative experimental results will be presented to demonstrate the effectiveness of the proposed control scheme.

5.2 Proposed Current Control Scheme

5.2.1 Modeling of Digital Control System of VSIs

For a DSP-based grid-connected VSI control system, modeling in z-plane is an easy and effective method to describe the system characteristics and analyze the system stability. Thus, a discrete model of VSIs needs to build firstly for the robust current controller design accounting for the nature of the inverter and sampling approximation. Recalling the averaged switch model discussed in Section 2.3.1, the output voltage of the inverter is assumed to remain constant during each switching cycle, thus, the inverter can be modeled as a sample-and-hold element, which can be represented by a zero-order hold (ZOH) circuit with a transfer function $G_0(s)$

$$G_0(s) = \frac{1-e^{-sT_s}}{s} \tag{5.1}$$

where T_s is the switching period.

Thus, the discrete model of the VSI can be illuminated by Fig. 5.1 and expressed as

$$\frac{i_g}{v_{ab}-\overline{V_g}} = Z\left\{G_0(s)\cdot\frac{1}{Ls}\right\} = \frac{T_s}{L}\frac{1}{z-1} \tag{5.2}$$

where v_{ab} is the output voltage of the inverter and $\overline{V_g}$ is the average grid voltage during the discretized sampling interval.

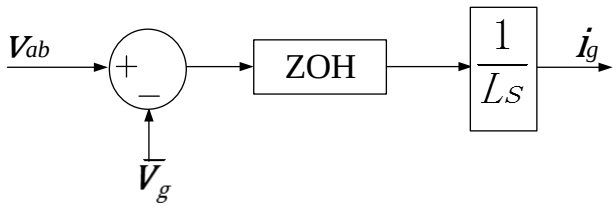


Fig. 5.1 Discrete model of VSIs with ZOH element

When the implemented switching frequency of VSIs is high, a linear extrapolation method is highly effective in compensating current and voltage errors caused by time delays, and thus the discrete-time predictive current controller can be seen as an ideal deadbeat digital current controller, whose control block diagram is presented in Fig. 5.2. It is clear that when the proportional gain of $\frac{L}{T_s}$ is applied and disturbances from the grid voltage estimation is assumed to be zero, the closed-loop transfer function for the plant shown in Fig. 5.2 is $\frac{1}{z}$ which achieves a fast unit delay current tracking with zero steady-state errors.

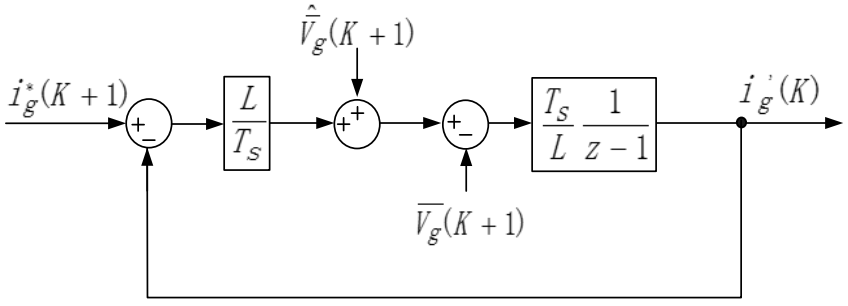


Fig. 5.2 Ideal predictive current controller

However, time-delay compensation by a linear predictor is only valid when the system dynamic characteristic is significantly slower than the delay time [125]. When the inverter operates at a lower switching frequency, the accuracy of predictive grid current and voltage obtained from equation (4.7) severely decreases which then results in degradation of system performance and stability. As seen from the experimental results of the grid current THD with the predictive controller summarized in Table 4.7, one can observe that the current harmonic distortion is higher than expected when the inverter operates at more than 5 kW and worsens as the switching frequency reduces, which illustrates that the predictive control based on a linear estimation is not able to realize a complete time-delay compensation when an inverter operates with a medium or low switching frequency. Furthermore, the variable operational switching frequency of the inverter under VSFC leads to undesirable and uncontrollable fluctuation in output performance of current harmonic distortion among the different work conditions due to uncertain time-delay effects with the linear prediction.

In order to overcome these limitations of the linear prediction method and enhance capability to attenuate the time-delay effect, a robust current control scheme with a new sampling strategy is proposed in this Section. Fig. 5.3 shows the new sampling scheme designed for the proposed robust current controller, where T_d denotes the inevitable part of time delays including the program calculation and the PWM update. In this research, $T_d = 20\ \mu s$. Consequently, the measurement of the actual current $i_g'(K)$ is selected at the sampling point $B(K)$ which is located in the period $[KT_s - T_d, KT_s - T_d - T_{ADC}]$ in order

to minimize the delay time as well as to keep the enough margins for operation, which is expressed by

$$i_g'(K) = i_B(K) \tag{5.3}$$

where $i_B(K)$ is the measured value of the actual current at the sampling point $B(K)$.

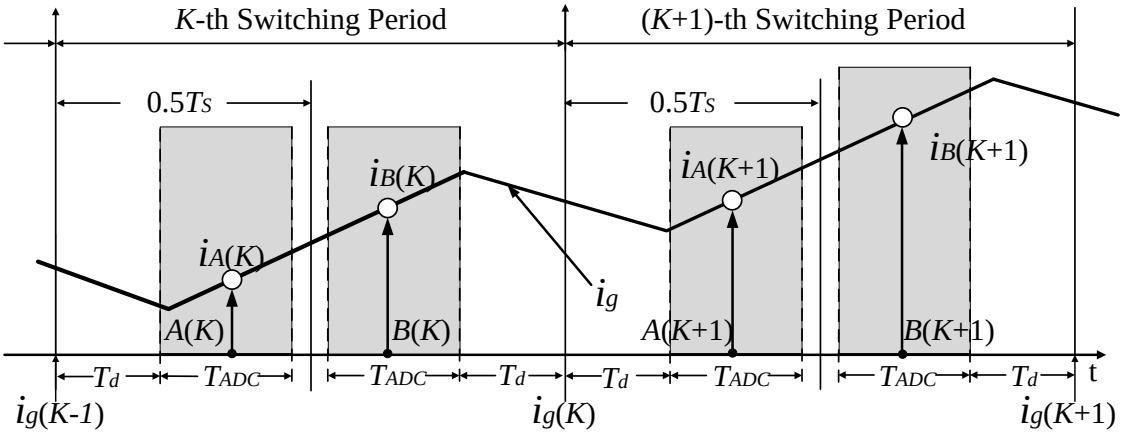


Fig. 5.3 Sampling strategy for robust current controller

In addition, the other sampling point during the K-th switching period is chosen in period of $[(K-1)T_s + T_d, (K-1)T_s + T_d + T_{ADC}]$, which is used to estimate the average grid voltage $\overline{v_g}(K)$ expressed by

$$\overline{v_g}(K) \approx \frac{v_{g\_A}(K) + v_{g\_B}(K)}{2} \tag{5.4}$$

where $v_{g\_A}(K)$ and $v_{g\_B}(K)$ are the measured grid voltage during the K-th switching period at the sampling points A and B, respectively.

As the grid frequency is much lower than the switching frequency, the assumption of a linear change of the grid voltage in two consecutive switching period is still used to predictive the average grid voltage in the $(K+1)$-th switching period

$$\hat{\overline{v_g}}(K+1) = 2\overline{v_g}(K) - \overline{v_g}(K-1) \tag{5.5}$$

The errors of the grid voltage originated from estimation by (5.4) will be considered as system disturbances and canceled by the proposed adaptive voltage compensator which will be discussed in Section 5.2.3.

According to the forgoing analysis, the new sampling scheme is effective to limit the sampling delay in a small range of T_d to $(T_d + T_{ADC})$. Moreover, the impact of time delays can be directly reflected in the control system diagram to evaluate the performance and stability of the current controller by a discrete model. Considering that the total delay time T_m determined by T_d and the sampling point distribution is less than the switching period (discretized sampling interval) and the delay influence lasts until the next switching cycle, the time delay can be regarded as a sample and linearly varying element, which can be represented by a first-order hold (FOH) circuit with a transfer function $G_1(s)$

$$G_1(s) = \frac{1}{1+sT_s} \tag{5.6}$$

Then, the z transform of the transfer function of the uncertain time delay e^{-sT_m} can be given by

$$G_d(z) = Z\{G_1(s) \cdot e^{-sT_m}\} = \frac{(1-K_d)z+K_d}{z} \tag{5.7}$$

where $K_d = \frac{T_m}{T_s}$.

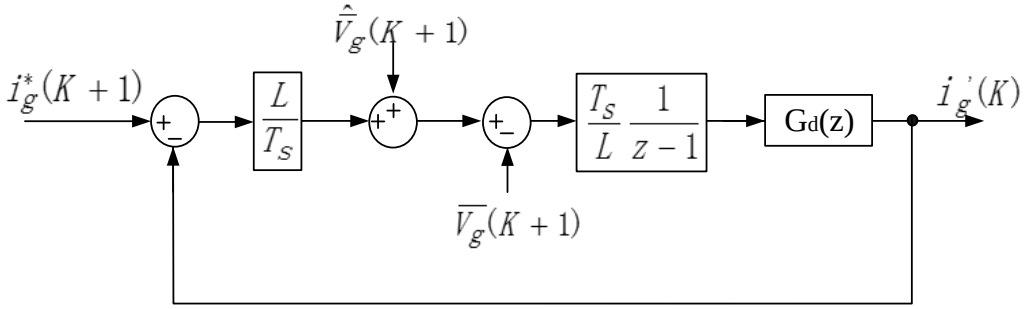


Fig. 5.4 Current control scheme with time-delay consideration

When the actual measured grid current $i_g'(K)$ is considered as the predictive current for the $(K+1)$-th switching cycle, the corresponding control scheme based on the new sampling system is shown in Fig. 5.4 and its closed-loop unit step response is illustrated in Fig. 5.5. It can be observed that the system dynamic performance is rapidly deteriorated in terms of both the percent overshoot and the settling time, as the delay time increases.

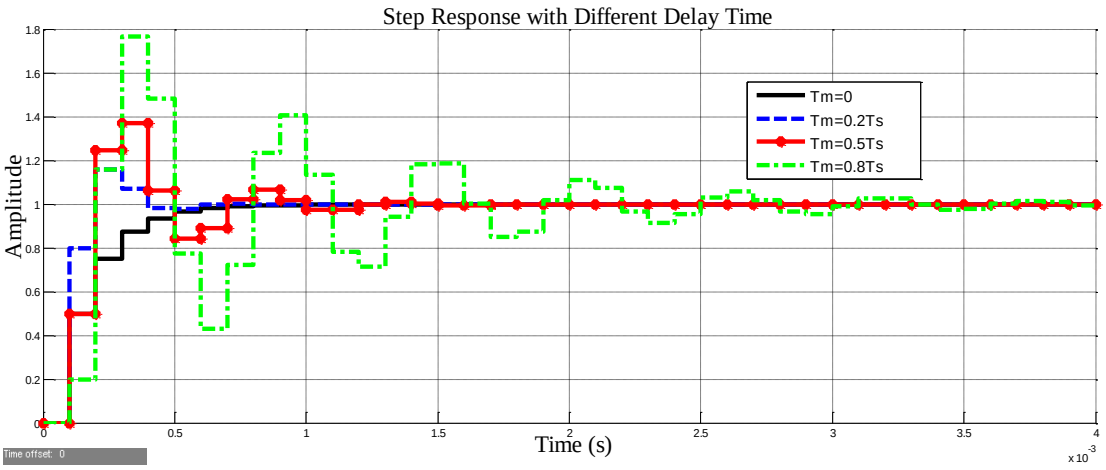


Fig. 5.5 Step responses of predictive current controller with different delay time

5.2.2 Weighted Filter Predictor

In order to compensate the effect of time-delays generated from the new sampling strategy, the current control system with a simple weighted filter predictor (WFP) is proposed in Fig. 5.6. Compared with the predictive current controller shown in Fig. 5.4, a weight factor m has been introduced to the current feedback loop to mitigate the tracking errors due to the sampling delay. The predictive current at the end point of the K-th switching period can be obtained by a weighted filter prediction method which is given as

$$\hat{\imath}_g(K) = mi'_g(K) + (1-m)i^*_g(K-1) \tag{5.8}$$

where $i^*_g(K-1)$ is reference current value for the $(K-1)$-th switching cycle and the weight factor $m \in (0,1]$.

With the new sampling scheme presented in Section 5.2.1, the weighted filter prediction method for the proposed robust current controller can be expressed by

$$\begin{cases} \hat{\imath}_g(K) = mi_B(K) + (1-m)i_g^*(K-1) \\ \hat{\bar{v}}_g(K+1) = \frac{1}{2}[2v_{g\_A}(K) + 2v_{g\_B}(K) - v_{g\_A}(K-1) - v_{g\_B}(K-1)] \end{cases} \tag{5.9}$$

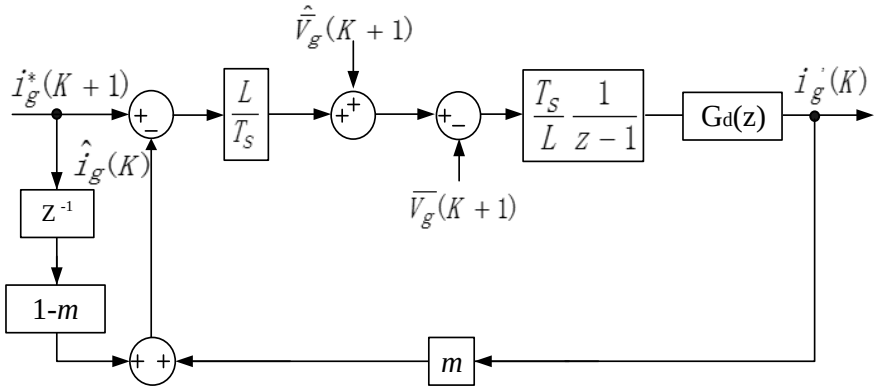


Fig. 5.6 Current control scheme with WFP

The factor m is used to determine the extent of robust error cancellation as well as the dynamic performance of current control scheme. A larger m renders a faster transient response, but a higher amplitude of the overshoot, and vice versa, as shown in Fig. 5.7. When a proper value of m is selected, the proposed WFP can reduce the current tracking error to approximate m times the original, while providing the enough information about transient characteristic of the feedback current. In this dissertation, m is set to 0.5, taking into account both compensation performance and system dynamics. Fig. 5.8 shows performance comparison of step responses of the predictive current controller with and without the time-delay compensation by the WFP, when $m = 0.5$ and $T_m = 0.5T_s$. The simulation result illustrates that the proposed WFP can provide a good compensation for time-delay effect featured in shorter settling time and lower overshoot amplitude.

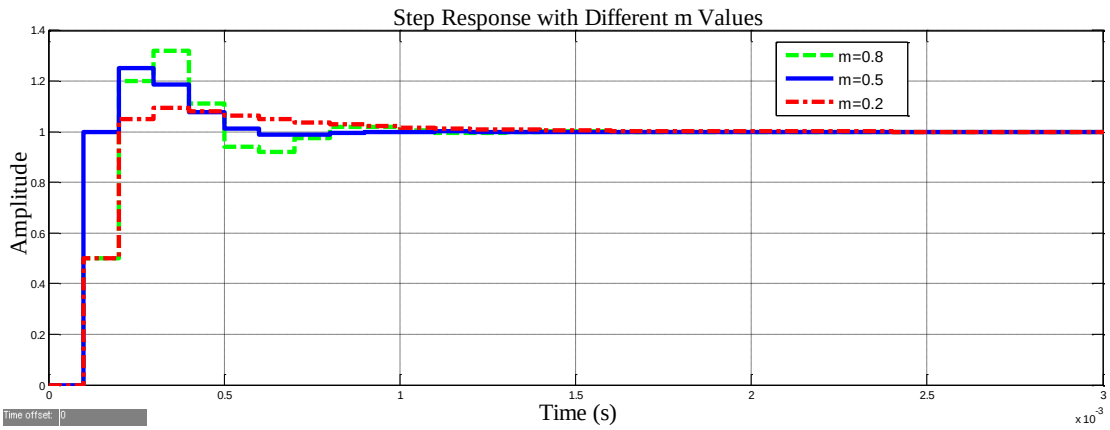


Fig. 5.7 Step Response of predictive current controller with WFP when m varies

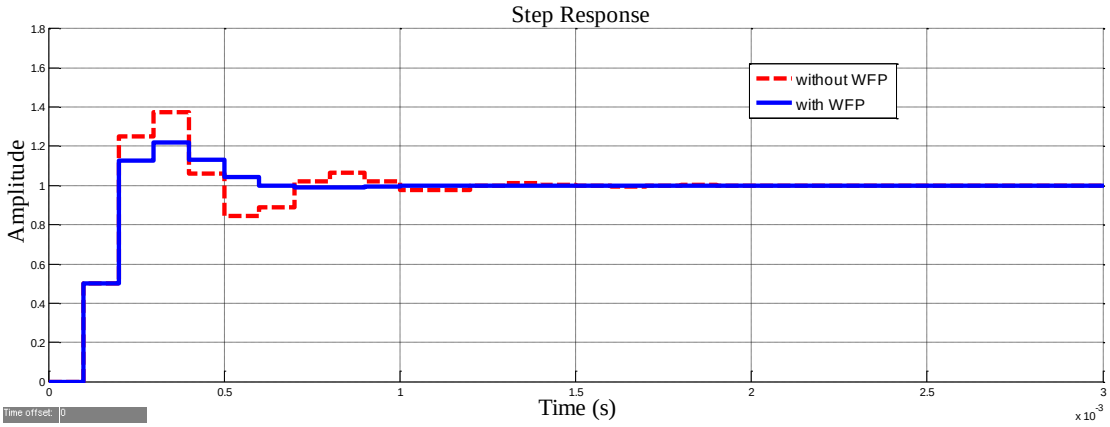


Fig. 5.8 Step responses of predictive current controller with and without WFP

5.2.3 Adaptive Voltage Compensator

Although the predictive current controller with WFP exhibits robust control performance for the time-delay effect, its underlying assumption is that the estimated grid voltage which acts as system disturbances is fully compensated by the linear estimation. However, when a linear prediction cannot provide the proper compensation for the grid voltage with a lower operational switching frequency, the existence of the voltage disturbance

can significantly affect the current tracking performance as well as increase the sensitivity of the current control scheme to system parameter variations. A steady-state error is shown on the plot in Fig. 5.9 as an example to indicate the effect of the disturbances on the output current, which displays a unit step response of the WFP-based current controller with a small grid voltage disturbance.

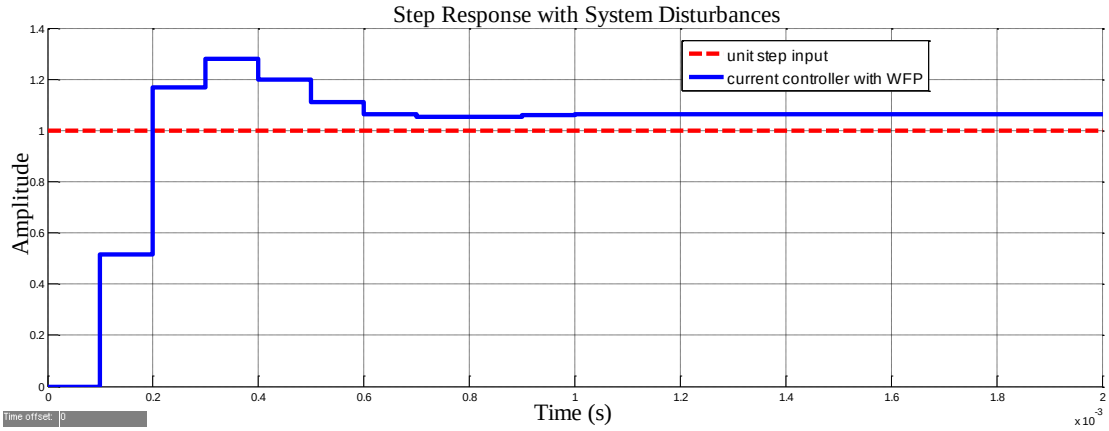


Fig. 5.9 Step responses of WFP-based controller with system disturbances

In addition, the mismatch of system parameter modeling can also result in uncertain disturbances in a practical grid-connected VSI system and aggravates the system performance and stability, such as the filter inductance. Thus, to relax the assumption of no disturbance existence, an adaptive voltage compensator (AVC) is designed in this Section to eliminate the steady-state errors caused by the system disturbances as well as enhance robustness of the system to parameter variations. As shown in Fig. 5.10, a voltage $\hat{\Delta}(K+1)$ has been added to the current control scheme as disturbance

compensation by the proposed AVC. As a result, the reference value of the output voltage of the inverter in the $(K+1)$-th switching period can be given by

$$v_{ab}^{*}(K+1)=\frac{L_m}{T_s}\left[i_g^{*}(K+1)-\hat{i}_g(K)\right]+\hat{\bar{v}}_g(K+1)+\hat{\Delta}(K+1) \tag{5.10}$$

where $\hat{i}_g(K)$ is derived from (5.8) and L_m is the modeling (or nominal) value of the filter inductance.

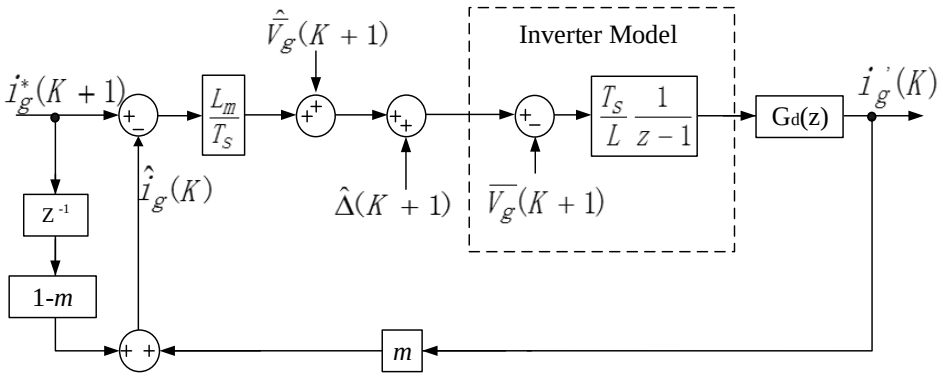


Fig. 5.10 WFP-based current control scheme with disturbance compensation

Assuming that the actual inverter output current is consistent with the reference one by a proper PWM technique, the operation of the grid-connected VSI can be expressed as

$$v_{ab}^{*}(K+1)=\frac{L}{T_s}\left[i_g(K+1)-\hat{i}_g(K)\right]+\bar{v}_g(K+1) \tag{5.11}$$

where $i_g(K+1)$ is the actual current at the end point of the $(K+1)$-th switching cycle and $\bar{v}_g(K+1)$ is the actual average value of the grid voltage during the $(K+1)$-th switching cycle.

When L_m is represented by $K_L L$, where K_L is the mismatch coefficient, (5.11) can be rewritten as

$$v_{ab}^*(K+1) = \frac{K_L L}{T_s}\left[i_g(K+1) - \hat{i}_g(K)\right] + \frac{(1-K_L)L}{T_s}\left[i_g(K+1) - \hat{i}_g(K)\right] + \bar{v}_g(K+1) \tag{5.12}$$

Solving (5.10) and (5.12) to obtain

$$\hat{\Delta}(K+1) - \left\{\left[\bar{v}_g(K+1) - \hat{\bar{v}}_g(K+1)\right] + \frac{(1-K_L)L}{T_s}\left[i_g(K+1) - \hat{i}_g(K)\right]\right\} = \frac{K_L L}{T_s}\left[i_g(K+1) - i_g^*(K+1)\right] \tag{5.13}$$

It is clear that the term of $\left\{\left[\bar{v}_g(K+1) - \hat{\bar{v}}_g(K+1)\right] + \frac{(1-K_L)L}{T_s}\left[i_g(K+1) - \hat{i}_g(K)\right]\right\}$ of (5.12) denotes the uncertain system disturbances due to the grid voltage estimation error and the filter inductance mismatch during the $(\mathrm{K}+1)$-th switching cycle, which can be represented by $\Delta(\mathrm{K}+1)$ in this dissertation. Hence, the difference between the estimated voltage compensation and actual system disturbances can be formulated as

$$\hat{\Delta}(K+1) - \Delta(\mathrm{K}+1) = \frac{K_L L}{T_s}\left[i_g(K+1) - i_g^*(K+1)\right] \tag{5.14}$$

From (5.14), the error between the reference value and actual current at the end of each switching period indicates the gap in the compensation for the system disturbances. Thus, a complete compensation for system disturbances can be achieved by an appropriate disturbance voltage adaptation algorithm with this current error.

Considering that the variation of the system disturbances in adjacent switching periods due to the high switching frequency applied, the uncertain system disturbances in the $(K+1)$-th switching period can be estimated by

$$\Delta(\mathrm{K}+1) \approx \Delta(\mathrm{K}) \tag{5.15}$$

Substituting (5.15) into (5.14) to yield

$$\hat{\Delta}(K+1) \approx \frac{K_L L}{T_s}\left[i_g(K+1) - i_g^*(K+1)\right] + \Delta(\mathrm{K}) = \frac{K_L L}{T_s}\left[i_g(K+1) - i_g^*(K+1)\right] +$$

$$\hat{\Delta}(K) - \frac{K_L L}{T_s}\left[i_g(K) - i_g^*(K)\right] \tag{5.16}$$

As current error between the actual measurement and reference value should be reduced progressively until rejected by the proposed iterating voltage compensation, $\left[i_g(K+1) - i_g^*(K+1)\right]$ can be defined as

$$i_g(K+1) - i_g^*(K+1) = \left[i_g(K) - i_g^*(K)\right] - \gamma\left[i_g(K) - i_g^*(K)\right] \tag{5.17}$$

where $\gamma \in (0,1)$. A larger value of γ can accelerate the convergence of the control system, but may result in system instability. In practice, γ is chosen as 0.1 in this dissertation.

Then, the disturbance compensation during the $(K+1)$-th switching period can be estimated by substituting (5.17) into (5.16) as

$$\hat{\Delta}(K+1) \approx \hat{\Delta}(K) - \frac{K_L L}{T_s}\gamma\left[\hat{\imath}_g(K) - i_g^*(K)\right] \tag{5.18}$$

where $i_g(K)$ is replaced by $\hat{\imath}_g(K)$ with WFP implementation.

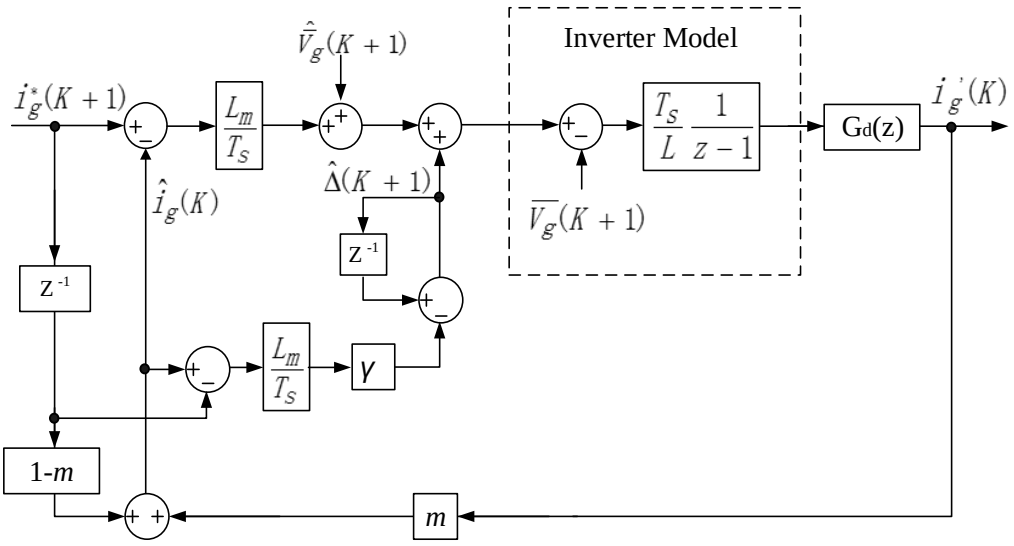


Fig. 5.11 Proposed robust current control scheme

Fig. 5.11 shows the proposed robust current control scheme with WFP and AVC. The AVC is developed based on the algorithm described in (5.18) which can be adopted to offer a complete voltage compensation for uncertain system disturbances. Fig. 5.12 and Fig. 5.13 show step responses of the proposed robust current controller with a small voltage disturbance and filter inductance mismatch, respectively. Compared with the traditional predictive controller without WFP and AVC, the simulation results illustrate that the proposed robust current control scheme is effective to reject the uncertain system disturbances and enhance the system robustness to parameter variations.

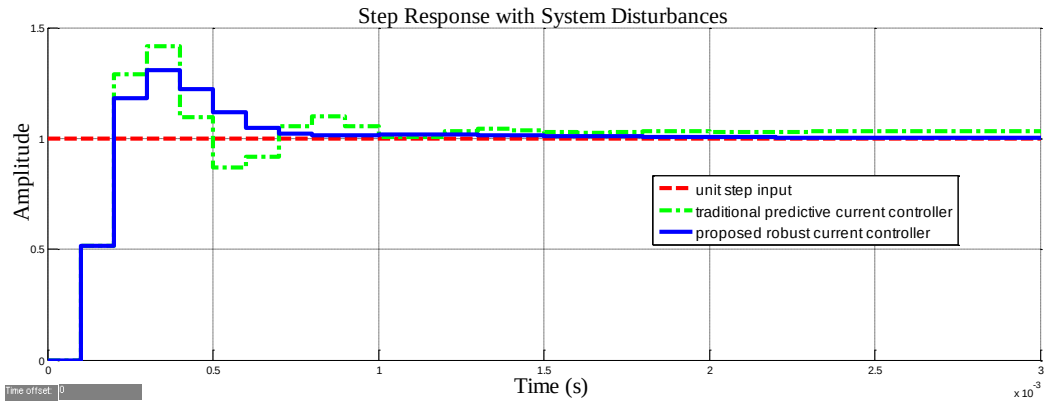


Fig. 5.12 Step response of proposed robust current controller with system disturbances

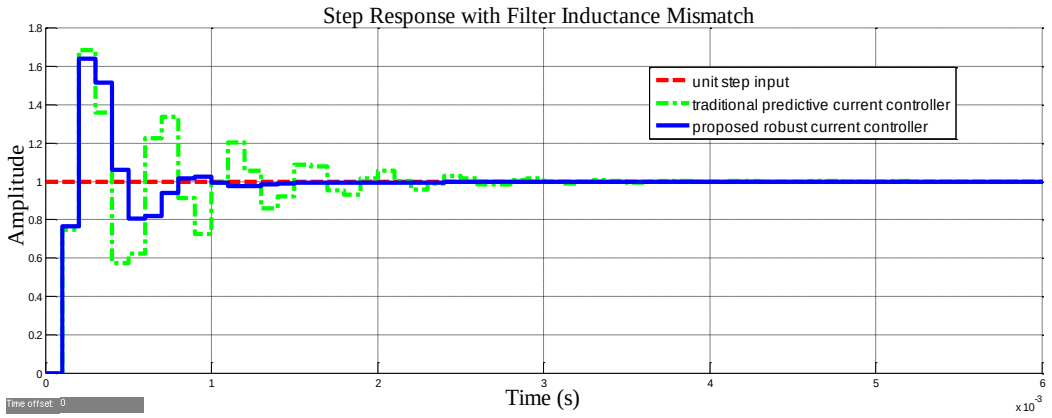


Fig. 5.13 Step response of proposed robust current controller with filter inductance mismatch (K_L=1.5)

5.3 System Stability Analysis

From Fig. 5.11, the grid voltage acting as system disturbance is assumed to be completely compensated by the proposed AVC, hence the analysis in this section is to concentrate on the system stability and robustness for the current loop within a filter inductance

mismatch. The closed-loop transfer function of the proposed current control scheme is given as

$$G_c(z) = \frac{(K_L-K_LK_d)z^3+(K_Lm-2K_L+K_Lm\gamma-K_LK_dm+3K_LK_d-K_LK_dm\gamma)z^2+(K_L-K_Lm-3K_LK_d+2K_LK_dm+K_LK_dm\gamma)z+K_LK_d-K_LK_dm}{z^4+(K_Lm+K_Lm\gamma-K_LK_dm-K_LK_dm\gamma-2)z^3+(1+2K_LK_dm+K_LK_dm\gamma-K_Lm)z^2-K_LK_dmz} \quad (5.19)$$

The Jury stability criterion [126] has been adopted in this Section to determinate the stability of the proposed control system by evaluating the coefficients of the system characteristic equation which is given by

$$F(z) = z^3 + (K_Lm + K_Lm\gamma - K_LK_dm - K_LK_dm\gamma - 2)z^2 + (1 + 2K_LK_dm + K_LK_dm\gamma - K_Lm)z - K_LK_dm \quad (5.20)$$

By definition, the Jury table of the proposed control system can be constructed as follows:

Table 5.1 Jury table for proposed control system

Row	z^0	z^1	z^2	z^3
1	$-K_LK_dm$	$1 + 2K_LK_dm + K_LK_dm\gamma - K_Lm$	$K_Lm + K_Lm\gamma - K_LK_dm - K_LK_dm\gamma - 2$	1
2	1	$K_Lm + K_Lm\gamma - K_LK_dm - K_LK_dm\gamma - 2$	$1 + 2K_LK_dm + K_LK_dm\gamma - K_Lm$	$-K_LK_dm$
3	$(K_LK_dm)^2 - 1$	$2 + K_LK_dm\gamma - (2+\gamma)(K_LK_dm)^2 - K_Lm + K_d(K_Lm)^2 - K_Lm\gamma$	$(1+\gamma)[(K_LK_dm)^2 - K_d(K_Lm)^2] + K_Lm - K_LK_dm\gamma - 1$	0

Thus, the system will be stable if all conditions shown in (5.21) are satisfied.

$$\begin{cases} F(1) > 0 \\ F(-1) < 0 \\ |-K_L K_d m| < 1 \\ |(1+\gamma)[(K_L K_d m)^2 - K_d(K_L m)^2] + K_L m - K_L K_d m\gamma - 1| < |(K_L K_d m)^2 - 1| \end{cases} \tag{5.21}$$

As satisfied K_L for a stable system indicates a consecutive range of filter inductance variations, when $m, \gamma \in (0,1)$ and $K_d \in (0,0.5)$ due to a maximum switching frequency of 10 kHz, solve (5.21) to obtain (see a detailed analysis in Appendix F)

$$K_L < \min\{\frac{4}{(2m+m\gamma)(1-2K_d)}, \frac{2}{m}, \frac{1-\mathrm{K_d}\gamma}{\mathrm{K_d}m(1+\gamma-\mathrm{K_d}\gamma)}\} \tag{5.22}$$

As the value of K_d varies in the range from almost zero to 0.5 under the VSFC, it can be found that $\frac{4}{(2m+m\gamma)(1-2K_d)}$ yields the minimum value when $K_d = 0$, while $\frac{1-\mathrm{K_d}\gamma}{\mathrm{K_d}m(1+\gamma-\mathrm{K_d}\gamma)}$ gets its minimum when $K_d = 0.5$. Thus, to stabilize the system with any time delay which is less than $0.5T_s$, the allowed K_L can be derived from (5.22) by evaluating the possible minimum value. As $\min\{\frac{1-\mathrm{K_d}\gamma}{\mathrm{K_d}m(1+\gamma-\mathrm{K_d}\gamma)}\} < \min\{\frac{4}{(2m+m\gamma)(1-2K_d)}\} < \frac{2}{m}$, K_L is chosen for the stable control system as

$$K_L < \frac{1-0.5\gamma}{0.5m(1+0.5\gamma)} \tag{5.23}$$

It is clear that lower values of m and γ can enhance the system robustness, however, reduce the system dynamic response. To achieve good quality in both robustness and fast response, values of m and γ are evaluated by practical experiments. In this dissertation, $m = 0.5$ and $\gamma = 0.1$. As a result, the system with the proposed current controller is stable for $0 < K_L \leq 3.6$. Compared with the traditional predictive controller shown in Fig.

5.4 or the linear predictive controller discussed in Chapter 4 with a stable range of $0 < K_L < 2$, the proposed control scheme significantly improves the system stability and robustness.

5.4 Evaluation Results

To verify the performance of proposed control scheme, experiments have been carried out on the same laboratory platform of 10 kW single-phase grid-connected inverter as that shown in Fig. 4.9 and the results have been evaluated by comparison with the linear predictive current controller presented in Chapter 4.

Fig. 5.14 shows the quality of the grid current when the inverter worked at 10 kW with a switching frequency of 3 kHz. It can be seen that the current THD under the linear prediction was 3.5%, higher than expectation by the THD estimation model, due to the amplified error of the current prediction caused by a lower switching frequency. However, the current quality was improved by the proposed robust current control scheme, which had a better THD of 2.8% shown in Fig. 5.14(b).

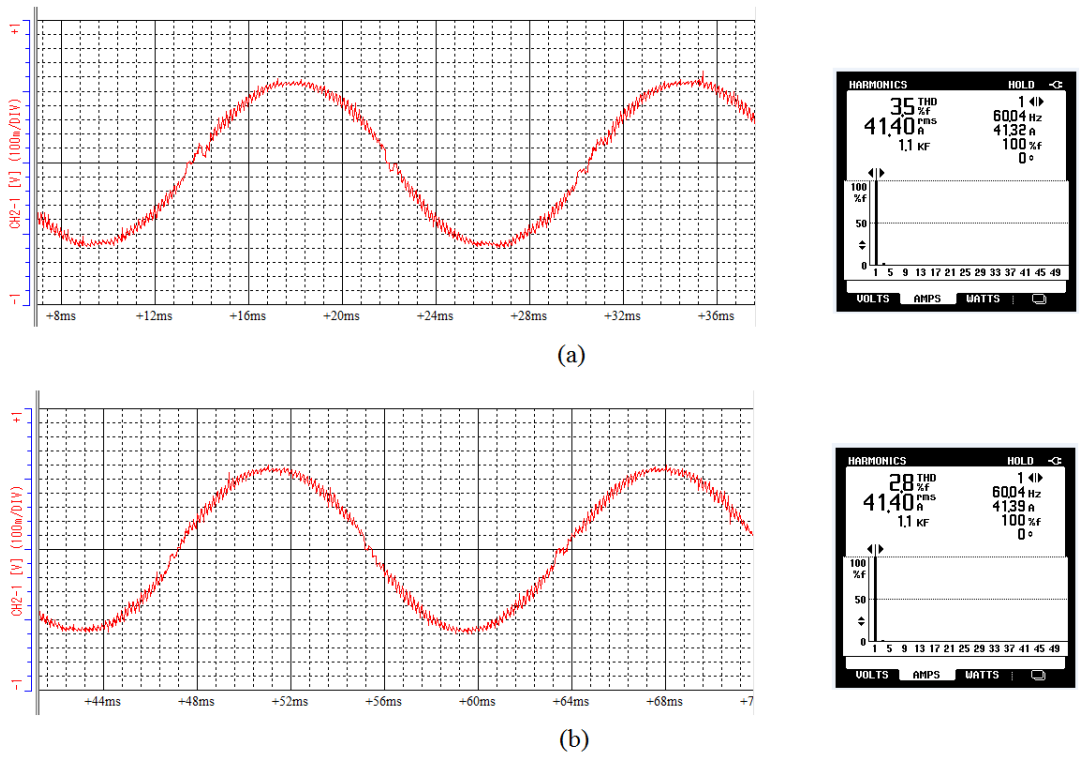


Fig. 5.14 Grid current waveform and THD performance at 10 kW (a) with linear predictive current control (b) with proposed robust current control

In addition, Fig. 5.15 and Fig. 5.16 illustrate the experimental comparison of the two current control schemes under the filter inductance mismatch conditions. When the inverter operated at 7 kW with a 10 kHz switching frequency, the modeling inductance of the filter L_m was set at five different values, which included the correct filter inductance L, $(1 \pm 20\%)L$ and $(1 \pm 50\%)L$. In Fig. 5.15 and Fig. 5.16, the scope measurements of grid current (i_g) were processed by a low pass filter with a cutoff frequency of 5 kHz for observation. The THDs of output grid current are summarized in Table 5.2, which indicate when $K_L < 1$ which means the modeling inductance is smaller than the actual one, two current control algorithms show comparable results, while when $K_L > 1$, the

proposed current control scheme exhibits a much better robustness characteristic for the filter inductance mismatch. This confirms the analysis in Section 5.3 and demonstrates the disturbance rejection property of the proposed control system.

And finally, a 4-min record of the grid current has been presented in Fig. 5.17 to evaluate the performance of the proposed robust current controller implemented for VSFC. With a preset THD requirement of 3%, an average of the THD measurements during an operation period of four minutes was 3.2% which is significantly improved compared with the result shown in Fig.4.10 by the linear predictive current controller. Furthermore, from Table 5.3 which details the THD quality at typical output power levels, it is clear that the VSFC algorithm is incorporated with the proposed robust current control scheme to achieve a low current harmonic and high efficiency performance of VSIs.

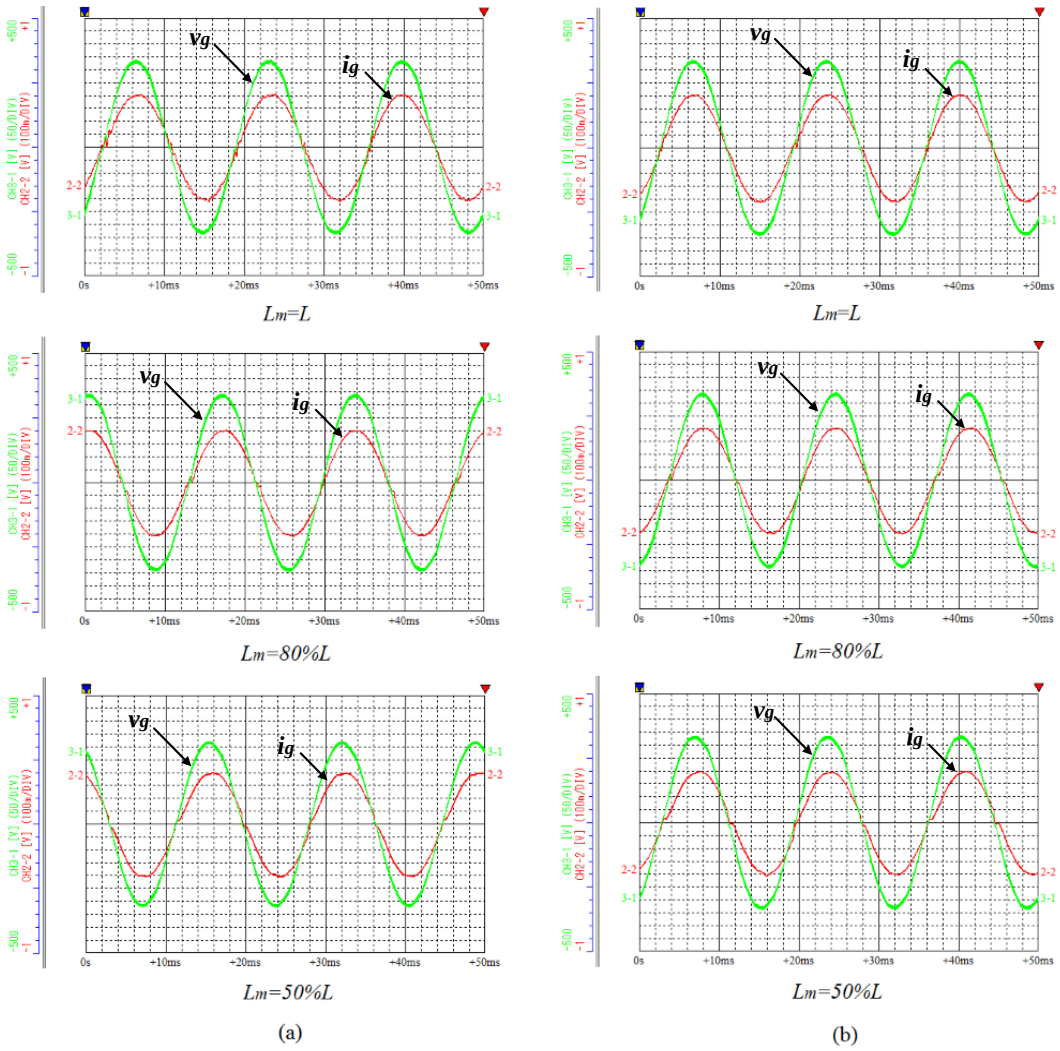


Fig. 5.15 Waveforms of grid current and voltage when $K_L \leq 1$ (a) with linear predictive current control (b) with proposed robust current control

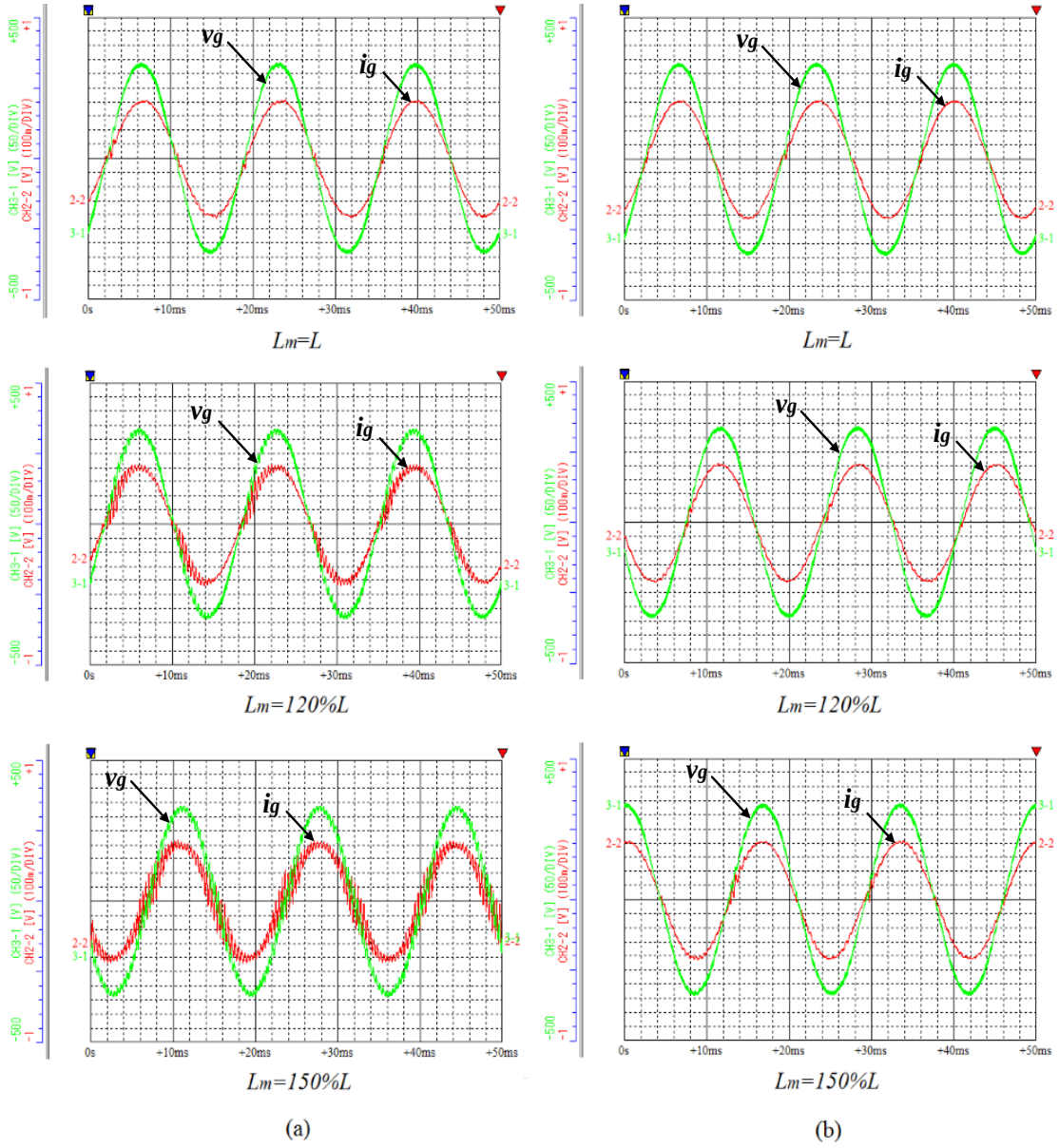


Fig. 5.16 Waveforms of grid current and voltage when $K_L \geq 1$ (a) with linear predictive current control (b) with proposed robust current control

Table 5.2 Grid current THDs with filter inductance mismatch

K_L	Current THD (%) with linear predictive controller	Current THD (%) with proposed robust controller
0.5	3.4	2.5
0.8	1.9	1.3
1	1.3	1.2
1.2	3.8	1.3
1.5	8.7	1.7

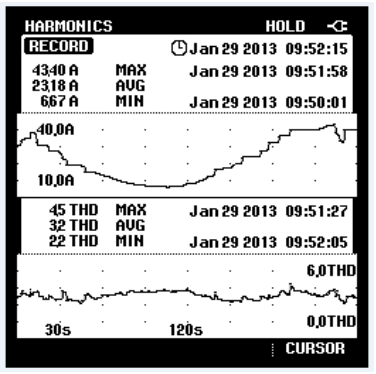


Fig. 5.17 Current THD record for 4-min operation under VSFC incorporated with proposed current control scheme

Table 5.3 Switching frequency and current THD of the inverter operating with proposed current controller for VSFC strategy

Output Power (kW)	Switching Frequency (kHz)	Current THD (%)
0.99	10.00	8.0
1.99	10.00	4.2
3.11	9.80	3.0
5.03	6.29	2.8
7.55	3.95	2.6
9.92	2.99	2.8

5.5 Summary

In this Chapter, a robust current control scheme is designed for grid-connected VSIs to improve the quality of the current fed to the grid as well as enhance the system stability and robustness. The proposed control scheme is developed from the traditional predictive current controller along with a WFP and an AVC. The WFP instead of the linear prediction method is primarily used to attenuate the amplified effect of time-delays when a low or medium switching frequency is applied. As for the AVC, it is implemented to provide a complete compensation for system disturbances which may include estimation errors for the grid voltage, variations of system parameters and etc. through an adaptive voltage control. Both theoretical analysis and experimental results have been presented in this Chapter to demonstrate the properties of the time-delay compensation and the disturbance rejection of the proposed current control scheme. In addition, when the VSFC algorithm is applied, the output performance of the inverter is significantly improved with the proposed current control scheme in terms of current harmonic distortion.

6 Conclusions and Future Work

6.1 Conclusions

This Ph.D. research investigated the efficiency improvement of small-scale single-phase grid-connected VSIs in wind and PV generation systems. The conclusions drawn from the studies were verified by both a Matlab-based simulation and an experimental platform of a 10 kW single-phase grid-connected VSI prototype.

Firstly, a loss analysis of VSIs was presented to clarify the power loss distribution of a VSI and identify the major factors in the efficiency improvement. An efficiency model of VSIs based on analytical expressions of VSI losses was built afterwards. By comparing the efficiencies of the VSI controlled by three typical modulation techniques including Unipolar SPWM control, CCPWM control and CCSVPWM control, reducing the operational switching frequency is considered as one of the most effective ways to improve the VSI efficiency.

Secondly, THD/ TDD prediction models of the grid current were proposed to evaluate power quality of VSI output under CCSVPWM control. The current harmonics in the full frequency range were estimated by the RMS value of a sum of current ripples based on the superposition theory and were confirmed by the Matlab-based simulation. Moreover, the low frequency components of current harmonics, as the main concern for compliance with grid interconnection standards were identified by deducting the high frequency harmonics from overall harmonic content obtained from the current ripple estimation,

which was verified by experimental results. In addition, reviewing both the expression of the THD/ TDD prediction models and experimental results of THD/ TDD of the grid current, one can obtain that the switching frequency of a grid-connected VSI as a crucial factor in output power quality has a direct effect on current harmonic distortion, where a higher switching frequency results in a lower current harmonic distortion.

Then, a new and effective algorithm called “VSFC” was developed to increase the total efficiency of grid-connected VSIs through choosing optimal switching frequencies in real time along with variations of operation conditions. The optimal switching frequencies were selected based on the efficiency estimation model and current harmonic perdition models to achieve a minimum of power losses and at the same time, satisfy the requirement of grid interconnection standards in terms of current harmonic distortion. According to the experimental results, the proposed VSFC strategy can improve the maximum efficiency of a 10 kW VSI by more than 0.8%, and European efficiency and the CEC efficiency by more than 0.5% without any change of hardware structure and inter-loop algorithm implementation.

Finally, a robust current controller was designed for grid-connected VSIs to improve the output power quality and system stability. Compared with the current controller with a linear predictor, the proposed control scheme exhibited a better current THD performance particularly when a lower switching frequency is applied, and higher robustness to system parameter mismatch through providing a compensation for time-delays and system disturbances.

6.2 Major Contributions

A simple and novel algorithm called variable switching frequency control has been developed, which can minimize the switching losses of grid-connected VSIs and at the same time comply with requirements of the utility interconnection standards. This method is highly effective in efficiency improvement for VSIs particularly for grid-connected renewable generation systems.

A mathematical model of current harmonic distortion based on the estimation of current ripples has been proposed to predict and evaluate the output power quality of VSIs with various working conditions and PWM techniques applied.

A robust current controller has been designed to achieve better current performance and higher system robustness for grid-connected VSIs. With the implementation of the developed weighted filter predictor and adaptive voltage compensator, the proposed robust current control scheme provides an effective compensation for time delays and system disturbances.

An efficiency model of VSIs has been proposed to estimate the power loss distribution of VSIs with different PWM techniques. The model is established based on analytical expressions of VSI losses including dc-link capacitor losses, on-state losses and switching losses of semiconductor devices and the filter losses.

6.3 Future Work

With VSFC, a grid-connected VSI operates with a range of optimal switching frequencies. As a result, the audible noise of VSIs may be aggravated under certain operating conditions when some harmonics move to an audible region. Thus, an optimization of the filter design is a worthy research topic in the future.

In addition, the proposed VSFC in this research can be implemented as a universal method to integrate with other advanced control algorithms for small-scale grid-connected VSIs in future to further improve the inverter efficiency without modifications in hardware design.

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Appendix A Matlab Code for Loss Distribution Estimation

```
%%%LOSS DISTRIBUTION CALCULATION %%%

clear;
clc;

%Switching frequency
C_m= input('Please type which modulation method you want to implement (1-SPWM, 2-CCPWM, 3-CCSVPWM): ');

%Switching frequency
f_s = input('Please Input The Switching Frequency: ');
T_s = 1/f_s;

%Grid frequency
f_0 = 60;
T_0 = 1/f_0;
w_0 = 2*pi*f_0;

%MPPT power
P_max = input('Please Input The MPPT Power You Want: ');
V_dc = input('Please Input The V_DC Voltage You Want: ');
I_in = P_max/V_dc;

%T_jection
T_j = input('Please Input T_j (Juntion Temperature): ');

%Parameters
Delta_t = T_s;
L = 1.6e-3;%input('Please Input The Choke Inductance: ');
V_grid_rms = 240;
V_grid = 2^0.5*V_grid_rms;
R_cap = 0.1212;

%%%Inductor loss%%%
%P_inductot_loss = P_iron + P_copper
%P_iron = P_hysteresis + P_eddy_current +P_extra
%followed equation: P_iron = a*f*B_ac^x + b*f^2*B_ac^2 +e*f^1.5*B_ac^1.5
%unit:(w/kg)
%a,b,x,c have different values based on different material

%for DW315-50
a = 0.022871;
b = 0.000004;
```

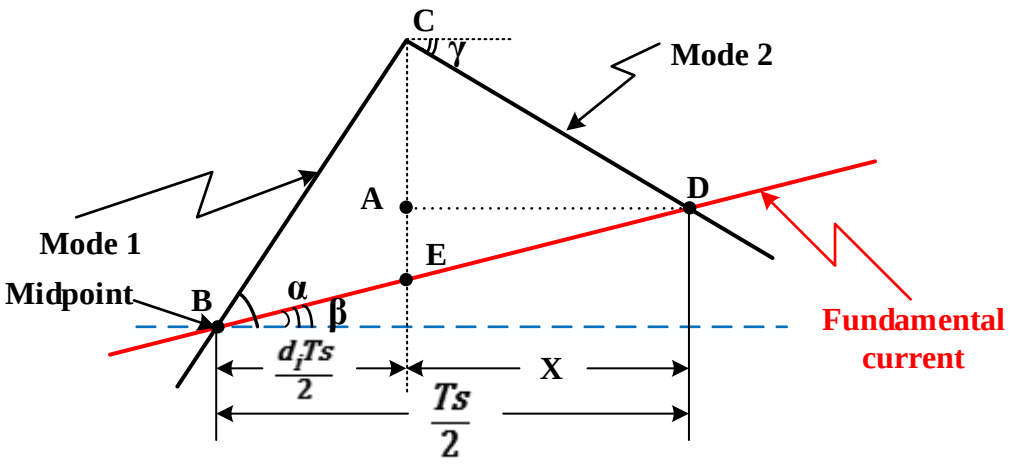
```
x = 1.685945;
e = 0.000588;
%parameter for the inductor, weight, Ae-effective cross-sectional area,N-turn
%number, copper resistance
V = 8;
N_t = 40;
Ac = 3e-3;
R_cu = 0.07;

%Test efficiency
% for i = 1:101
% P_max = 1e2*(i-1);

I_c_rms = P_max/V_grid_rms;
I_c = 2^0.5*I_c_rms;

%The  switching times in [0 Pi]
% n = T_0/(2*T_s);
n = T_0/T_s;
N = ceil(n/2);

%Temp variables
IGBT_LOSS = zeros(2,1);
FS_V_PWM = zeros(2,40);

%Initial value
I_sensor = 0;
t_03 = 0;
t_3 = 0;
d_k_old = 1;


for k = 1:N
        t_k = k*T_s-0.5*T_s;

%% averaged switch model

        I_c_k = I_c*sin(w_0*t_k);
        V_grid_k = V_grid*sin(w_0*t_k);

%% duty cycle

        %SPWM
        if C_m == 1
           M = (2*V_grid_rms^2+2*(w_0*L*I_c_rms)^2)^0.5/V_dc;
```

```
        d_k = M*sin(w_0*t_k);
        d_1_k = 1;
        d_4_k = d_k;
        d_d2_k = 0;
        d_d3_k = 1-d_k;
        N_equ = 1; %equ number of switching idbts
    end

    %CCPWM
    if C_m == 2
        d_k = (V_grid*sin(w_0*t_k)+L*(I_c*sin(w_0*(t_k+0.5*T_s))-
                I_c*sin(w_0*(t_k-0.5*T_s)))/Delta_t)/V_dc;
        d_1_k = 1;
        d_4_k = d_k;
        d_d2_k = 0;
        d_d3_k = 1-d_k;
        N_equ = 1;
    end

    %CCSVPWM
    if C_m == 3
        d_k = (V_grid*sin(w_0*t_k)+L*(I_c*sin(w_0*(t_k+0.5*T_s))-
                I_c*sin(w_0*(t_k-0.5*T_s)))/Delta_t)/V_dc;
        d_1_k = 0.5+0.5*d_k;
        d_4_k = 0.5+0.5*d_k;
        d_d2_k = 0.5-0.5*d_k;
        d_d3_k = 0.5-0.5*d_k;
        N_equ = 2;
    end

    %0<= d_k <= 1
    if d_k > 1 d_k = 1; end
    if d_k < 0 d_k = 0; end

%% DC-link loss
    I_cap_k_2 = I_in^2+d_k*I_c_k^2-2*d_k*I_in*I_c_k; %I_cap_k_2 = I_cap_k^2;
    W_cap_k = I_cap_k_2*R_cap*T_s;

%% IGBT & Diode loss

    % on-state loss
    V_ce_k = 1+0.015*I_c_k+(0.2+0.004*I_c_k)*(T_j-25)/100;
    V_f_k = 1.3+0.01*I_c_k+0.005*(T_j-25);

    W_igbt_k =  V_ce_k*I_c_k*T_s*(d_1_k+d_4_k);
```

```
        W_diode_k =  V_f_k*I_c_k*T_s*(d_d3_k+d_d2_k );

        % switching loss
        E_sw_on_k = V_dc/600*(2.3+0.12*I_c_k)*1e-3;
        E_sw_off_k = V_dc/600*(1.8+0.09*I_c_k)*1e-3;
        E_sw_k = N_equ*(E_sw_on_k+E_sw_off_k);

%% inductor loss

      %copper loss
      % P_cu = I_c_rms^2*R_cu;  % for whole grid period

      %iron loss
       delta_B_k = 0.5*((V_dc-V_grid_k)*d_k*T_s+(-V_grid_k)*(1-d_k)*T_s);
       d_B_k =  (V_dc-V_grid_k)^2*d_k*T_s+(-V_grid_k)^2*(1-d_k)*T_s;

       t(k) = t_k;
      d(k) = d_k;
      W_cap(k) = W_cap_k;
      W_igbt(k) = W_igbt_k;
      W_diode(k) = W_diode_k;
      E_sw(k) = E_sw_k;
      % W_iron(k) =  W_iron_k;
      delta_B(k) = delta_B_k;
      B_2_f(k) = d_B_k;

end

P_cap = sum(W_cap)/(N*T_s)
P_igbt = sum(W_igbt)/(N*T_s)
P_diode = sum(W_diode)/(N*T_s)
P_sw = sum(E_sw)/(N*T_s)
%P_iron = sum(W_iron)/(N*T_s)
B_max= sum(delta_B);
B_2 = sum(B_2_f);
P_iron = V*(a*f_0/(Ac*N_t)*B_max^x + b/(n*T_s)/(N_t*Ac)^2*B_2)
P_cu = I_c_rms^2*R_cu

%efficieny
E = 1-(P_cap+P_igbt+P_diode+P_sw+P_cu+P_iron)/P_max
```

Appendix B Proof of a Prerequisite for Ripple Current Calculation

In order to prove that if the current at the middle point of each switching cycle is selected as the reference current, the initial point and the final point of the actual current in each switching period are on the curve of the fundamental current when both a proper current control algorithm and a unit power factor are applied, the current waveform shown in the below can be analyzed by geometrical methods.



According to the averaged switch model of the inverter, when a proper current control algorithm and a unit power factor are applied, $\tan\alpha$, $\tan\beta$ and $\tan\gamma$ can be represented by

$$\begin{cases} \tan\alpha = \frac{1}{L}\left(V_{dc} - \overline{v_{g\_i}}\right) \\ \tan\beta = \frac{1}{L}\left(d_i V_{dc} - \overline{v_{g\_i}}\right) \\ \tan\gamma = -\frac{\overline{v_{g\_i}}}{L} \end{cases}$$

From the point of geometry, we can obtain that

$$\overline{CE} = \overline{CA} + \overline{AE}$$

$$\because \begin{cases} \overline{CE} = \frac{d_i T_s}{2}(\tan\alpha - \tan\beta) \\ \overline{CA} = x(-\tan\gamma) \\ \overline{AE} = x\tan\beta \end{cases}$$

$$\therefore \frac{d_i T_s}{2}(\tan\alpha - \tan\beta) = x(\tan\beta - \tan\gamma)$$

Solving the equation to obtain

$x = \frac{(1-d_i)T_s}{2}$, that demonstrates that the point D shown in the figure is the final point of the actual current in each switching period.

The initial point of the actual current in each switching period can be proved on the curve of the fundamental current by the same method due to symmetric PWM control.

Appendix C Estimation of the RMS current ripple

According to (3.21)

$$\Delta I_{g_{RMS}} = \frac{V_{dc}T_sC_1}{4\sqrt{3}L}\sqrt{\frac{1}{\pi}\int_0^{\pi}\left({C_2}^2 - 2C_1{C_2}^3 + {C_1}^2{C_2}^4\right)d(\omega_0 t)}$$
$$= \frac{V_{dc}T_sC_1}{4\sqrt{3\pi}L}\sqrt{A}$$

where $C_1 = \frac{\sqrt{2{V_g}^2+2(L\omega_0 I_{ref})^2}}{V_{dc}}$, $\varphi = \tan^{-1}\frac{L\omega_0 I_{ref}}{V_g}$ and

$$A = \int_0^{\pi}\left\{[\sin(\omega_0 t+\varphi)]^2 - 2C_1[\sin(\omega_0 t+\varphi)]^3 + {C_1}^2[\sin(\omega_0 t+\varphi)]^4\right\}d(\omega_0 t)$$

We have

$$\int_0^{\pi}[\sin(\omega_0 t+\varphi)]^2\,d(\omega_0 t) = \frac{\omega_0 t+\varphi}{2} - \frac{\sin(2\omega_0 t+2\varphi)}{4}\Big|_0^{\pi}$$
$$= \frac{\pi}{2}$$

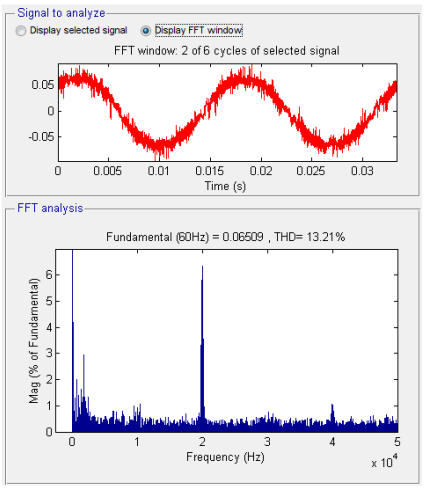
$$\int_0^{\pi} -2C_1[\sin(\omega_0 t+\varphi)]^3\,d(\omega_0 t) = -\frac{C_1}{6}[\cos 3(\omega_0 t+\varphi) - 9\cos(\omega_0 t+\varphi)]\Big|_0^{\pi}$$
$$= -\frac{C_1}{3}[12\cos\varphi - 4(\cos\varphi)^3]$$

$$\int_0^{\pi}{C_1}^2[\sin(\omega_0 t+\varphi)]^4\,d(\omega_0 t) = \{{C_1}^2[\frac{3}{8}(\omega_0 t+\varphi) - \frac{1}{4}\sin2(\omega_0 t+\varphi)$$
$$+\frac{1}{16}\sin4(\omega_0 t+\varphi)\}\Big|_0^{\pi}$$
$$= \frac{3\pi}{8}{C_1}^2$$

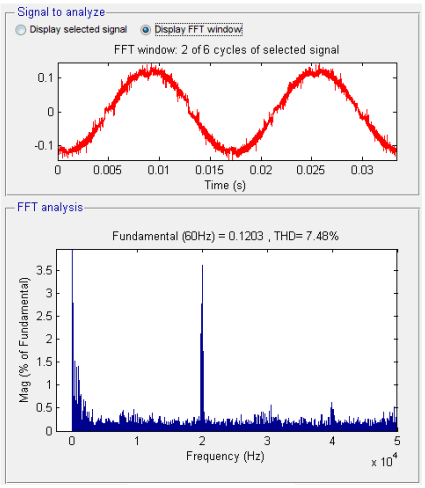
Thus,

$$\begin{aligned}
\Delta I_{g_{RMS}} &= \frac{V_{dc}T_sC_1}{4\sqrt{3\pi}L}\cdot\sqrt{\frac{\pi}{2}-\frac{C_1}{3}[12\cos\varphi-4(\cos\varphi)^3]+\frac{3\pi}{8}{C_1}^2} \\
&= \frac{T_s}{24\sqrt{2\pi}LV_{dc}}\cdot[36\pi{V_g}^4+72\pi{V_g}^2\left(L\omega_0 I_{ref}\right)^2+36\pi\left(L\omega_0 I_{ref}\right)^4 \\
&\quad +24\pi{V_{dc}}^2{V_g}^2+24\pi{V_{dc}}^2\left(L\omega_0 I_{ref}\right)^2-128\sqrt{2}V_{dc}{V_g}^3 \\
&\quad -192\sqrt{2}V_{dc}V_g\left(L\omega_0 I_{ref}\right)^2]^{\frac{1}{2}}
\end{aligned}$$

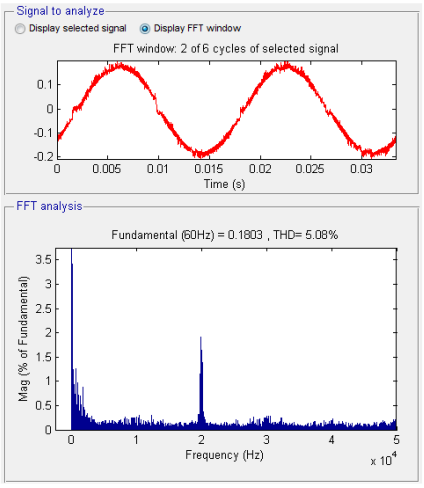
Appendix D Current Harmonic Analyses in Matlab



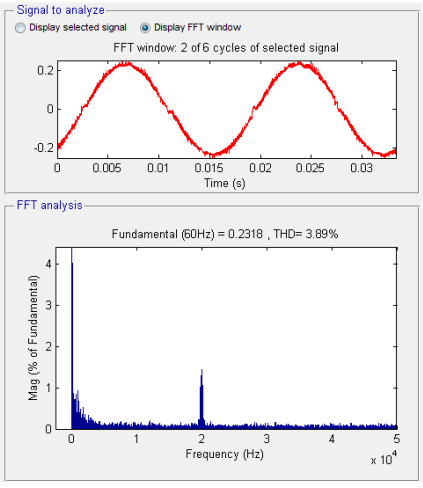
Operation at 1kW



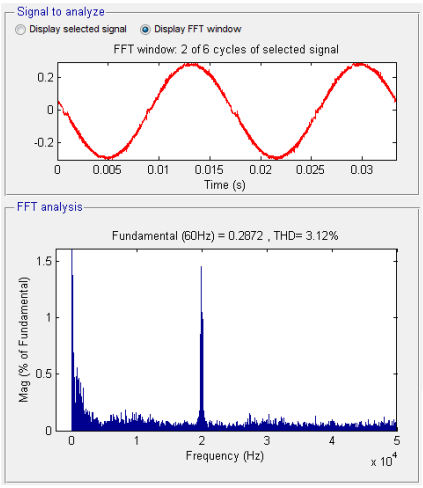
Operation at 2kW



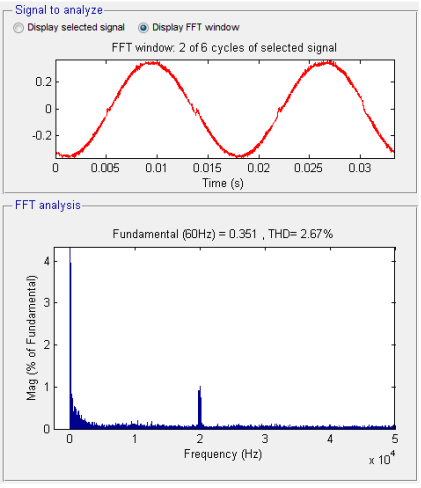
Operation at 3kW



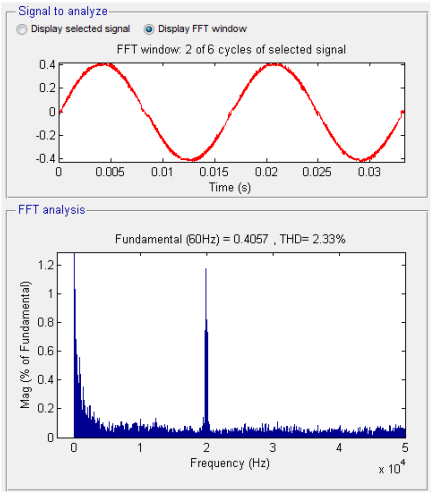
Operation at 4kW



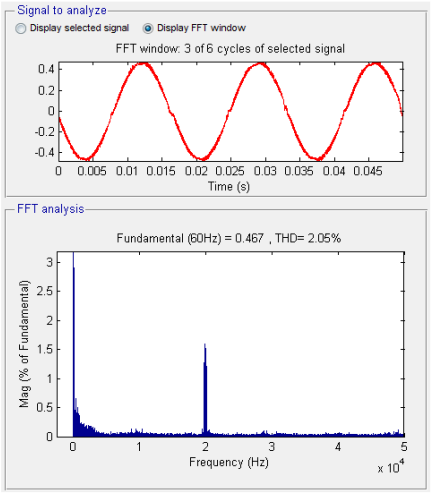
Operation at 5kW



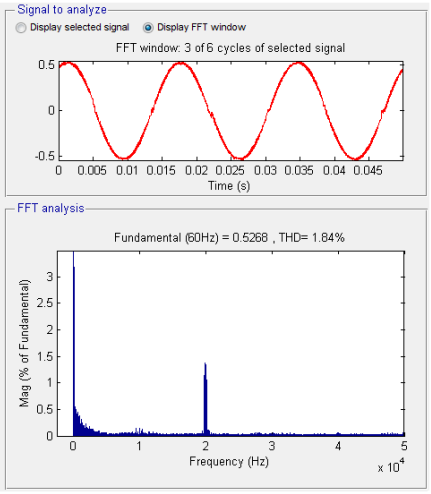
Operation at 6kW



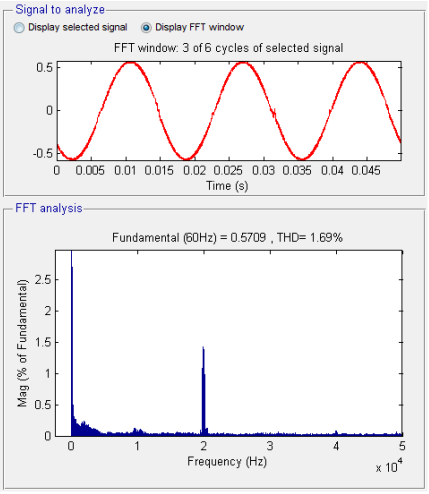
Operation at 7kW



Operation at 8kW



Operation at 9kW



Operation at 10kW

Appendix E Solution of (3.33) by Using a Taylor Series

A solution for "$\int_0^{\pi} \sin(A\sin x)\cdot\sin x\,dx$" is presented firstly by using a Taylor series, where $A = \frac{\sqrt{2}V_g\pi}{V_{dc}}$.

$$\sin(A\sin x) = \sum_{k=0}^{\infty} \frac{(-1)^k A^{2k+1}}{(2k+1)!}(\sin x)^{2k+1}$$

$$\sin(A\sin x)\cdot\sin x = \sum_{k=0}^{\infty} \frac{(-1)^k A^{2k+1}}{(2k+1)!}(\sin x)^{2k+2}$$

$$\int_0^{\pi} \sin(A\sin x)\cdot\sin x\,dx = \sum_{k=0}^{\infty} \frac{(-1)^k A^{2k+1}}{(2k+1)!}\int_0^{\pi}(\sin x)^{2k+2}\,dx$$

Note that $\int_0^{\pi}(\sin x)^{2k+2}\,\mathrm{dx} = \pi\frac{(2k+1)\cdot(2k-1)\cdot(2k-3)\cdots3\cdot1}{(2k+2)\cdot(2k)\cdot(2k-2)\cdots4\cdot2} = \pi\frac{(2k+1)!!}{(2k+2)!!}$ for any non-negative integer k.

Then,

$$\begin{aligned}\int_0^{\pi} \sin(A\sin x)\cdot\sin x\,dx &= \pi\sum_{k=0}^{\infty}\frac{(-1)^k A^{2k+1}}{(2k+1)!}\frac{(2k+1)!!}{(2k+2)!!}\\ &= \pi\sum_{k=0}^{\infty}\frac{(-1)^k A^{2k+1}}{(2k)!!\,(2k+2)!!}\\ &= \pi\sum_{k=0}^{\infty}\frac{(-1)^k A^{2k+1}}{2^{(2k+1)}k!\,(k+1)!}\end{aligned}$$

where $\sum_{k=0}^{\infty}\frac{(-1)^k A^{2k+1}}{2^{(2k+1)}k!(k+1)!}$ is exactly the definition of the Bessel function of $J_1(A)$. As a result,

$$\int_0^{\pi} \sin(A \sin x) \cdot \sin x \, dx = \pi J_1(A)$$

Thus,

$$\frac{-8V_{dc}\omega_0}{\pi\omega_s} \cdot \frac{1}{\omega_0 T_s} \int_0^{\pi} \sin\left(\frac{\sqrt{2}V_g\pi}{V_{dc}} \sin x\right) \cdot \sin x \, dx = \frac{-2V_{dc}}{\pi} J_1\left(\frac{\sqrt{2}V_g\pi}{V_{dc}}\right)$$

where $\omega_s = \frac{4\pi}{T_s}$.

Appendix F Stability Analysis by Jury Stability Criterion

When $m, \gamma \in (0,1)$ and $K_d \in (0,0.5]$, solve (5.21) to obtain

(1) $F(1) > 0$

Any value is satisfied, as $F(1) = K_L m\gamma > 0$;

(2) $F(-1) < 0$

$\Longrightarrow F(-1) = K_L(2m + m\gamma)(1 - 2K_d) < 0$

When $K_d \leq 0.5$, $K_L < \frac{4}{(2m+m\gamma)(1-2K_d)}$;

(3) $|-K_L K_d m| < 1$

$\Longrightarrow K_L K_d m < 1$, when $K_L, K_d, m \geq 0$

$\Longrightarrow K_L < \frac{2}{m}$, as $K_d \leq 0.5$;

(4) $|(1+\gamma)[(K_L K_d m)^2 - K_d(K_L m)^2] + K_L m - K_L K_d m\gamma - 1| < |(K_L K_d m)^2 - 1|$

A. When $(1+\gamma)[(K_L K_d m)^2 - [K_d(K_L m)^2] + K_L m - K_L K_d m\gamma - 1 < 0$,

$-\{(1+\gamma)[(K_L K_d m)^2 - K_d(K_L m)^2] + K_L m - K_L K_d m\gamma - 1\} - [1 - (K_L K_d m)^2] < 0$

should be satisfied.

We have

$(1+\gamma)[(K_L K_d m)^2 - [K_d(K_L m)^2] + K_L m - K_L K_d m\gamma - 1 < (1+\gamma)[(K_L K_d m)^2 -$

$[K_d(K_L m)^2] + K_L m - K_L K_d m\gamma - K_L K_d m$ when $K_L K_d m < 1$

Solve $(1+\gamma)[(\mathrm{K_L K_d m})^2 - [\mathrm{K_d}(\mathrm{K_L m})^2] + \mathrm{K_L m} - \mathrm{K_L K_d m}\gamma - \mathrm{K_L K_d m} < 0$ to yield $\mathrm{K_L} > \frac{1-\mathrm{K_d}\gamma-\mathrm{K_d}}{\mathrm{K_d}m(1+\gamma)(1-\mathrm{K_d})} = \frac{1-\mathrm{K_d}\gamma-\mathrm{K_d}}{\mathrm{K_d}m(1+\gamma-\mathrm{K_d}\gamma-\mathrm{K_d})}$, which indicates the existence of $\mathrm{K_0}$ which is less than $\frac{1-\mathrm{K_d}\gamma-\mathrm{K_d}}{\mathrm{K_d}m(1+\gamma-\mathrm{K_d}\gamma-\mathrm{K_d})}$ to satisfy $(1+\gamma)[(\mathrm{K_L K_d m})^2 - [\mathrm{K_d}(\mathrm{K_L m})^2] + \mathrm{K_L m} - \mathrm{K_L K_d m}\gamma - 1 < 0$.

Then, solve $-\{(1+\gamma)[(\mathrm{K_L K_d m})^2 - \mathrm{K_d}(\mathrm{K_L m})^2] + \mathrm{K_L m} - \mathrm{K_L K_d m}\gamma - 1\} - [1 - (\mathrm{K_L K_d m})^2] < 0$ to obtain

$(1+\gamma)\mathrm{K_d}(\mathrm{K_L m})^2 - (\mathrm{K_L K_d m})^2\gamma - \mathrm{K_L m} + \mathrm{K_L K_d m}\gamma < 0$

$\Longrightarrow K_L < \frac{1-\mathrm{K_d}\gamma}{\mathrm{K_d}m(1+\gamma-\mathrm{K_d}\gamma)}$

As $\frac{1-\mathrm{K_d}\gamma-\mathrm{K_d}}{\mathrm{K_d}m(1+\gamma-\mathrm{K_d}\gamma-\mathrm{K_d})} < \frac{1-\mathrm{K_d}\gamma}{\mathrm{K_d}m(1+\gamma-\mathrm{K_d}\gamma)}$, this condition can be satisfied when

$\mathrm{K_0} < K_L < \frac{1-\mathrm{K_d}\gamma}{\mathrm{K_d}m(1+\gamma-\mathrm{K_d}\gamma)}$

B. When $(1+\gamma)[(\mathrm{K_L K_d m})^2 - [\mathrm{K_d}(\mathrm{K_L m})^2] + \mathrm{K_L m} - \mathrm{K_L K_d m}\gamma - 1 \geq 0$,

$(1+\gamma)[(\mathrm{K_L K_d m})^2 - \mathrm{K_d}(\mathrm{K_L m})^2] + \mathrm{K_L m} - \mathrm{K_L K_d m}\gamma - 1 - [1 - (\mathrm{K_L K_d m})^2] < 0$

should be satisfied.

One can obtain

$(1+\gamma)[(K_L K_d m)^2 - K_d(K_L m)^2] + K_L m - K_L K_d m\gamma - 1 - [1 - (K_L K_d m)^2] =$

$K_L m - K_d(K_L m)^2(1+\gamma) - K_L K_d m\gamma + (K_L K_d m)^2\gamma - 2[1 - (K_L K_d m)^2]$

As $K_L K_d m < 1$, $1 - (K_L K_d m)^2 > 1 - K_L K_d m$,

$K_L m - K_d (K_L m)^2 (1+\gamma) - K_L K_d m\gamma + (K_L K_d m)^2 \gamma - 2[1 - (K_L K_d m)^2] < K_L m - K_d (K_L m)^2 (1+\gamma) - K_L K_d m\gamma + (K_L K_d m)^2 \gamma - 2(1 - K_L K_d m) = K_L m - K_d (K_L m)^2 - K_d (K_L m)^2 \gamma - K_L K_d m\gamma (1 - K_L K_d m) - 2(1 - K_L K_d m) = K_L m(1 - K_L K_d m) - K_d (K_L m)^2 \gamma - K_L K_d m\gamma (1 - K_L K_d m) - 2(1 - K_L K_d m) = (K_L m - 2)(1 - K_L K_d m) - K_d (K_L m)^2 \gamma - K_L K_d m\gamma (1 - K_L K_d m)$

When $K_L \leq \frac{2}{m}$, $(K_L m - 2)(1 - K_L K_d m) - K_d (K_L m)^2 \gamma - K_L K_d m\gamma (1 - K_L K_d m) < 0$.

As $\frac{2}{m} > \frac{1 - K_d \gamma}{K_d m(1+\gamma - K_d \gamma)} > K_0$, this condition can be satisfied if

$K_L \geq K_0$

Therefore, when $K_L < \frac{1 - K_d \gamma}{K_d m(1+\gamma - K_d \gamma)}$, the condition

$|(1+\gamma)[(K_L K_d m)^2 - K_d (K_L m)^2] + K_L m - K_L K_d m\gamma - 1| < |(K_L K_d m)^2 - 1|$ for Jury stability criterion is satisfied.

Curriculum Vitae

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Publications:

(1) Bo Cao and Liuchen Chang, "Robust Predictive Current Control for Grid-Connected VSIs with compensation for Time-Delay Effect and Uncertain System Disturbances," in *the 7th Annual IEEE ECCE*, 2015. Under revision.

(2) Bo Cao, Liuchen Chang and Riming Shao, "A Simple Approach to Current THD

Prediction for Small-Scale Grid-Connected Inverters," in *the 30th Annual IEEE APEC*, 2015. Accepted in October 2014.

(3) Bo Cao and Liuchen Chang, "A Variable Switching Frequency Algorithm to Improve the Total Efficiency of Single-Phase Grid-Connected Inverters," in *the 28th Annual IEEE APEC*, 2013, pp. 2310-2315.

(4) Yang Hu, Liuchen Chang and Bo Cao, "Novel Predictive Voltage Controller UPS inverter for an Improved Stand-Alone Wind Turbine System," in *CCECE*, 2009, pp. 398-402.

(5) Bo Cao, Liuchen Chang and Howard Li, "Implementation of the RBF Neural Network on a SOPC for Maximum Power Point Tracking," in *CCECE*, 2008, pp. 981-986.